

# ZSSC3286

## IO-Link Ready Dual Channel Resistive Sensor Signal Conditioner IC

The ZSSC3286 is a dual path sensor signal conditioning IC (SSC) for highly accurate amplification, digitization, and sensor-specific correction of sensor signals.

The ZSSC3286 supports IO-Link connectivity with an integrated IO-Link stack running the IO-Link Smart Sensor Profile for digital measuring and switching sensors.

The device is suitable for bridge and half-bridge sensors, as well as external voltage source elements.

Digital compensation of the sensor offset, sensitivity, temperature drift, and nonlinearity is accomplished via a 32-bit ARM based math core running a correction algorithm with calibration coefficients stored in a non-volatile, reprogrammable memory.

The programmable, integrated sensor front-end allows optimally applying various sensors for a broad range of applications.

The ZSSC3286 supports system calibration and firmware update via the IO-Link or I2C interface.

### Applications

- Industrial sensors with IO-Link interface
- Smart and digital sensors for energy-efficient solutions
- Single/Dual/Differential sensing
- Factory automation
- Process automation
- Calibrated, continuously operating sensors for:
  - Pressure
  - Flow
  - Load
  - Level
  - Temperature

### Features

- IO-Link stack embedded
- Smart Sensor Profile in COM3 mode
- Firmware update via IO-Link
- Calibration and configuration via IO-Link
- Clock recovery system, no external crystal needed
- IODD generator included
- Accommodates nearly all resistive bridge sensors in various configurations:
  - Resistive bridge or half-bridge
  - Resistive divider string
  - Voltage source
- On-chip temperature sensor
- External temperature sensing supported
- Programmable 16-bit digital-to-analog-converter and output (supporting “True-0Volt”-output):
  - Absolute voltage output (supporting 0V to 1V, 0V to 5V, or 0V to 10V applications)
  - 4mA to 20mA current-loop output supported
- Wide operational temperature and supply range
- On-chip voltage regulators for sensor supply, and IC operation
- Programmable sensor-signal-conditioning math core
- Reprogrammable, non-volatile memory (NVM)
- On-chip diagnostics:
  - Sensor connection
  - AFE self-test
  - Memory integrity

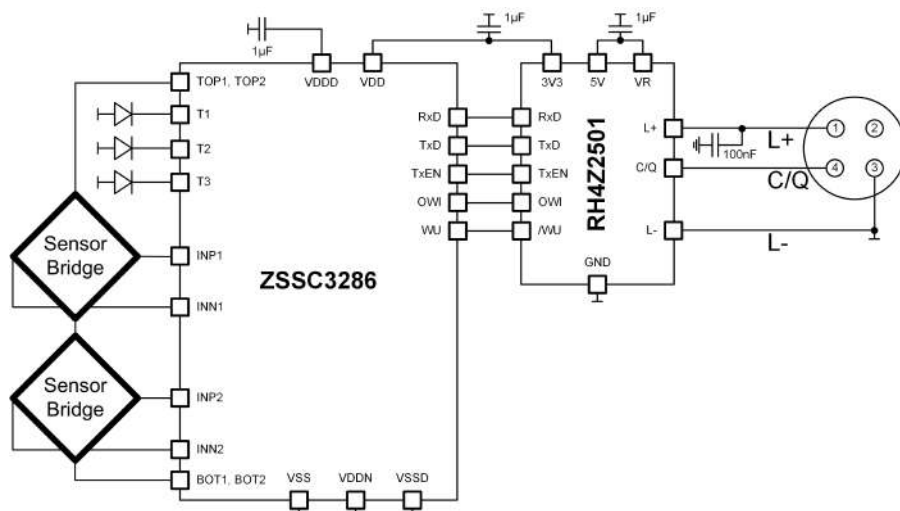


Figure 1: Typical Application Diagram

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# 1 Overview

## 1.1 Block Diagram

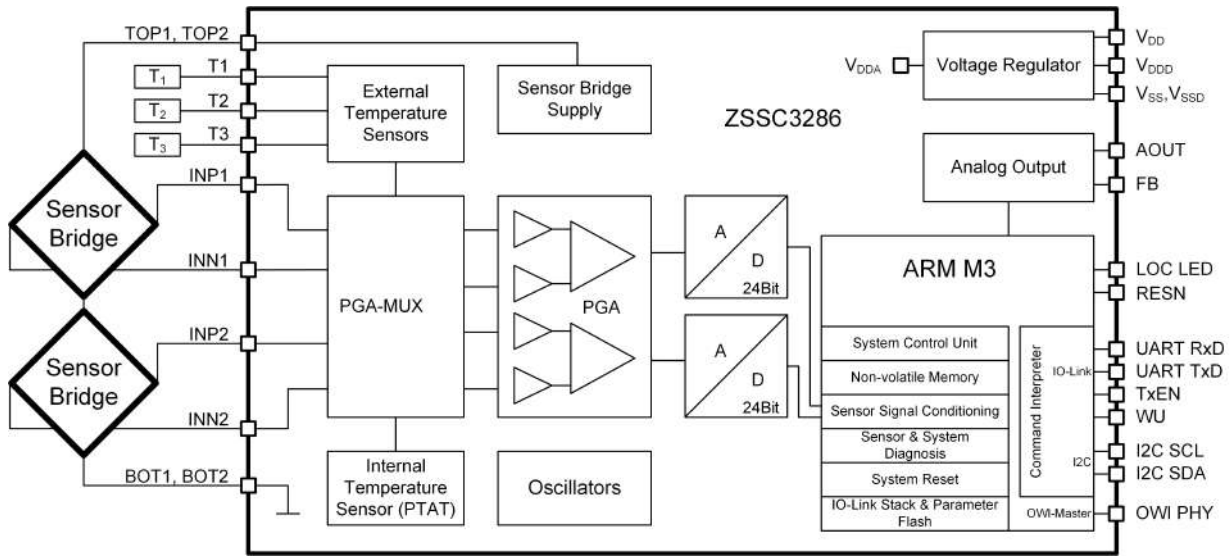
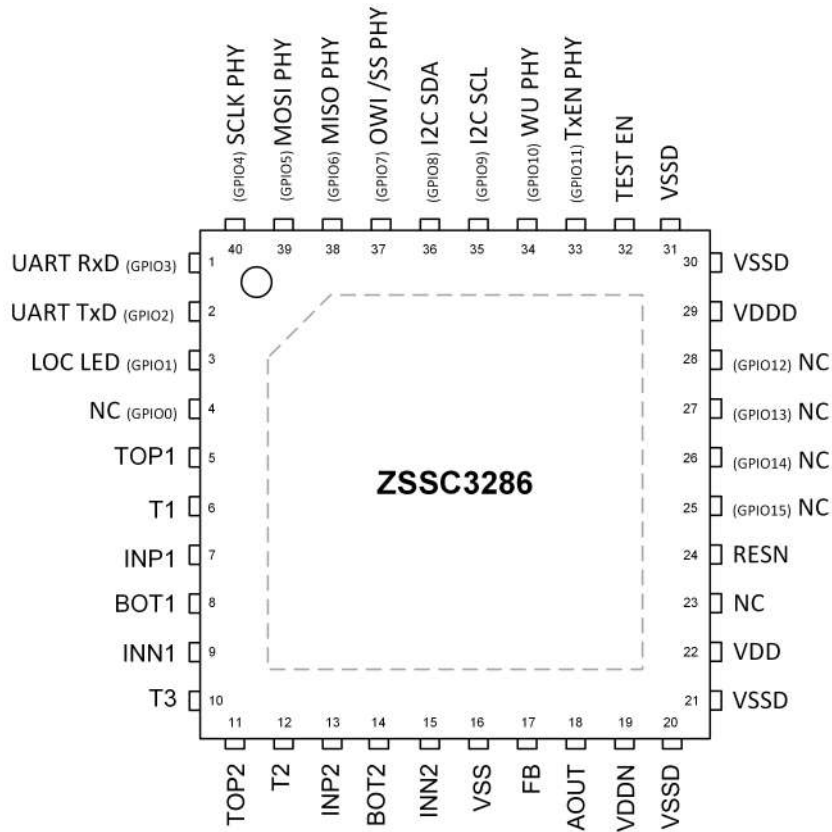


Figure 2: Block Diagram

## 1.2 Ordering Information

| Orderable Part Number | Description and Package  | MSL Rating | Carrier Type | Temperature Range |
|-----------------------|--|------------|--------------|-------------------|
| ZSSC3286BI3R          | 5 x 5 mm2 NDG40S1 (40-VFQFPN)  | MSL1       | 13 inch Reel | -40°C to 125°C    |
| ZSSC3286BI8R          | 3.57 x 3.12 mm2 WLCSP  | MSL1       | 13 inch Reel | -40°C to 125°C    |
| ZSSC3286KIT           | Modular ZSSC3286 SSC Evaluation Kit including three interconnecting boards, five ZSSC3286 QFN40 samples, one RH4Z2501 PMOD, one two channel IO-Link master and cable. Software is available for download on <a href="http://www.renesas.com/ZSSC3286">www.renesas.com/ZSSC3286</a> . |            |              |                   |

### 1.3 Pin Configuration



-----  
QFN-bottom plate, exposed pad.

Figure 3: Pin Layout QFN40



Figure 4: Pin Layout WLCSP

## 1.4 Pin Descriptions

| QFN40 Pin Number | Name        | Type                 | Description  |
|------------------|-------------|----------------------|--|
| 1                | UART RxD    | Digital Input        | GPIO3: UART receive function for IO-Link PHY communication   |
| 2                | UART TxD    | Digital Output       | GPIO2: UART transmit function for IO-Link PHY communication  |
| 3                | LOC LED     | Digital Output       | GPIO1: Timer functionality for Locator LED   |
| 4                | NC          | Digital Input/Output | GPIO0: Not connected. Leave pin floating.  |
| 5                | TOP1        | Analog Input/Output  | Positive sensor (bridge 1) supply or sensor-signal input   |
| 6                | T1          | Analog Input/Output  | External temperature sensor  |
| 7                | INP1        | Analog Input/Output  | Positive sensor (bridge 1) signal  |
| 8                | BOT1        | Analog Input/Output  | Sensor (bridge 1) ground or sensor-signal input  |
| 9                | INN1        | Analog Input/Output  | Negative sensor (bridge 1) signal  |
| 10               | T3          | Analog Input/Output  | External temperature sensor 3  |
| 11               | TOP2        | Analog Input/Output  | Positive sensor (bridge 2) supply or sensor-signal input   |
| 12               | T2          | Analog Input/Output  | External temperature sensor 2  |
| 13               | INP2        | Analog Input/Output  | Positive sensor (bridge 2) signal  |
| 14               | BOT2        | Analog Input/Output  | Sensor (bridge 2) ground or sensor-signal input  |
| 15               | INN2        | Analog Input/Output  | Negative sensor (bridge 2) signal  |
| 16               | VSS         | Ground               | Power supply ground  |
| 17               | FB          | Analog Output        | Feedback pin for AOUT. No connection if not used.  |
| 18               | AOUT        | Analog Output        | Analog smart-sensor output signal  |
| 19               | VDDN        | Analog Output        | Negative voltage output, charge pump buffer capacitor  |
| 20               | VSSD        | Ground               | Digital power supply ground  |
| 21               | VSSD        | Ground               | Digital power supply ground  |
| 22               | VDD         | Supply               | Power supply   |
| 23               | NC          | Analog Output        | Not connected. Leave pin floating.   |
| 24               | RESN        | Digital Input        | Digital IC reset (low active); internal pull-up  |
| 25               | NC          | Digital Input/Output | GPIO15: Not connected. Leave pin floating.   |
| 25               | NC          | Digital Input/Output | GPIO14: Not connected. Leave pin floating.   |
| 27               | NC          | Digital Input/Output | GPIO13: Not connected. Leave pin floating.   |
| 28               | NC          | Digital Input/Output | GPIO12: Not connected. Leave pin floating.   |
| 29               | VDDD        | Analog I/O           | Buffer cap connection for internal VDDD  |
| 30               | VSSD        | Ground               | Digital power supply ground  |
| 31               | VSSD        | Ground               | Digital power supply ground  |
| 32               | TEST EN     | -                    | Renesas internal use only. Connect to VSSD   |
| 33               | TxE PHY     | Digital Output       | GPIO11: UART transmit enable function for IO-Link PHY communication  |
| 34               | WU PHY      | Digital Output       | GPIO10: Wake-Up for IO-Link PHY communication  |
| 35               | SCL         | Digital Input        | GPIO9: I2C SCL   |
| 36               | SDA         | Digital Input/Output | GPIO8: I2C SDA   |
| 37               | OWI /SS PHY | Digital Input/Output | GPIO7: OWI master interface or Slave Select for IO-Link PHY communication  |
| 38               | MISO PHY    | Digital Input        | GPIO6: SPI master function - MISO for IO-Link PHY communication  |
| 39               | MOSI PHY    | Digital Output       | GPIO5: SPI master function - MOSI for IO-Link PHY communication  |
| 40               | SCLK PHY    | Digital Output       | GPIO4: SPI master function - Clock for IO-Link PHY communication   |
|                  | exposed pad | -                    | QFN-bottom plate, Die-bottom/substrate.<br>Recommendation is to connect to VSS, PAD to be used for heat dissipation and additional EMC robustness. |

## 2 Specifications

### 2.1 Absolute Maximum Ratings

| Symbol        | Parameter  | Conditions  | Minimum | Maximum | Units |
|---------------|--|---|---------|---------|-------|
| $T_J$         | Junction temperature   |   |         | 135     | °C    |
| $T_S$         | Storage temperature  |   | -45     | 150     | °C    |
|               | ESD: Human Body Model tested per JS-001-2017                     | Pins: INPx, INNx, TOPx, BOTx, Tx, VDDD                |         | 2000    | V     |
|               |  | Pins: GPIOx, VDD, VDDN, VSS, VSSD, AOUT, FB, RESN, NC |         | 4000    | V     |
|               | ESD: Charged Device Model tested per JS-002-2014 (OFN package)   | All Pins  |         | 750     | V     |
|               | ESD: Charged Device Model tested per JS-002-2014 (WLCSP package) | All Pins  |         | 500     | V     |
|               | Latch-up   | Tested per JESD78E; Class 2, Level A                  | -100    | +100    | mA    |
| $V_{DD\_max}$ | Maximum allowed for voltage supply                               | Referenced to VSS                                     | -0.3    | 6.5     | V     |
| $V_{IF\_max}$ | Voltage at digital I/O   | Referenced to VSSD                                    | -0.3    | 5.5     | V     |

**WARNING:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

### 2.2 Thermal Information

| Symbol        | Parameter | Conditions                           | Typical | Units |
|---------------|-----------|--------------------------------------|---------|-------|
| $\theta_{JA}$ | Theta JA  | 40Ld 5×5 QFN Package, 0 m/s air flow | 25.8    | K/W   |
|               |           | 40Ld 5×5 QFN Package, 1 m/s air flow | 22.4    | K/W   |
|               |           | 40Ld 5×5 QFN Package, 2 m/s air flow | 20.8    | K/W   |
| $\theta_{JB}$ | Theta JB  | 40Ld 5×5 QFN Package                 | 1.3     | K/W   |
| $\theta_{JC}$ | Theta JC  | 40Ld 5×5 QFN Package                 | 24.4    | K/W   |

### 2.3 Recommended Operating Conditions

| Symbol             | Parameter   | Minimum | Typical | Maximum | Units |
|--------------------|---|---------|---------|---------|-------|
| $V_{DD}$           | Power supply voltage  | 1.8     | -       | 5.5     | V     |
|                    | Flash write/erase   | 2.7     |         |         |       |
|                    | With optional "True-0V" at analog output  | 2.7     |         |         |       |
| $T_J$              | Junction temperature  | -40     |         | 125     | °C    |
| $C_{VDD}$          | External capacitance between VDD and VSS  | 10 ±20% |         | 22 ±20% | µF    |
| $C_{V3D}$          | External capacitance between VDDD and VSS   | 1 ±20%  |         | 1 ±20%  | µF    |
| $C_{VDDN}$         | External capacitance between VDDN and VSS, with optional "True-0V" at analog output                     | 1 ±20%  |         | 1 ±20%  | µF    |
| $C_{TOP\_EMC}$     | Recommended, external capacitance between TOP and VSS for electro-magnetic immunity (EMI)               | 0       | 6.8     | 8       | nF    |
| $C_{AOUT\_EMC}$    | Recommended, external capacitance between AOUT versus VDD and VSS for EMI suppression <sup>1</sup>      | 0       | 22      | 33      | 7nF   |
| $I_{Sensor}$       | Load current through external sensor element <sup>2</sup>   | 0.005   | 0.5     | 2       | mA    |
| $V_{DioDrop}$      | External temperature diode and RTD input range, drop over external element referenced to T1, T2, T3 pin | 0.2     |         | 1.2     | V     |
| $V_{Sens\_in}$     | Absolute sensor signal input level, INN, INP pins   | 0.2     |         | 1.2     | V     |
| $I_{max\_AOUT\_V}$ | Maximum current load at AOUT pin for voltage outputs  | 0       | 5       |         | mA    |
| $SR_{VDD\_POR}$    | Recommended VDD rise slew rate for Power-On-Reset (POR)   | 1.5     |         |         | V/ms  |
| $I_{max\_GPIO}$    | Maximum overall GPIO driver strength  |         |         | 120     | mA    |

<sup>1</sup> For applications with OWI interface or analog voltage output.

<sup>2</sup> With ratiometric sensor supply configuration. For example, a ratiometric bridge or bridge as temperature sensor with internal or external temperature sensitive resistor

## 2.4 Electrical Specifications

All parameter values are valid only under operating conditions specified in subsection 2.3. All voltages are referenced to VSS.

**Table 1: IC Supply**

| Symbol   | Parameter  | Conditions                          | Minimum | Typical | Maximum | Units |
|----------|--|-------------------------------------|---------|---------|---------|-------|
| $I_{IC}$ | Current consumption, active mode (depending on settings) | Excluding connected sensor elements |         | 8       | 15      | mA    |
| VDDA     | Internally generated analog supply                       |                                     | 1.6     | 1.65    | 1.85    | V     |

**Table 2: Sensor Supply**

| Symbol                 | Parameter  | Conditions   | Minimum | Typical | Maximum | Units      |
|------------------------|--|--|---------|---------|---------|------------|
| TOP                    | Sensor bias voltage in ratiometric Supply Mode                       | Ratiometric sensor voltage supply  |         | VDDA    |         | V          |
| $I_{bias\_TOP}$        | Sensor bias current used in Source Mode                              | Programmable in 10 steps:<br>0 $\mu$ A, 5 $\mu$ A, 10 $\mu$ A, 20 $\mu$ A, 40 $\mu$ A, 80 $\mu$ A, 100 $\mu$ A, 160 $\mu$ A, 200 $\mu$ A, 500 $\mu$ A  | 0       |         | 500     | $\mu$ A    |
| $I_{biasN\_BOT}$       | Sensor current used in Sink Mode                                     | Programmable in 2 steps:<br>20 $\mu$ A, 100 $\mu$ A  | 20      |         | 100     | $\mu$ A    |
| $I_{ERR}$              | Relative bias current ( $I_{bias\_TOP}$ and $I_{biasN\_BOT}$ ) error | Overall  | -10     |         | 10      | %          |
|                        |  | Over temperature range   | -1      |         | 1       |            |
| $R_{TH}, R_{TL}$       | TOP/BOT bias resistor  | Programmable in 12 steps:<br>open, 1k $\Omega$ , 33k $\Omega$ , 2k $\Omega$ , 4k $\Omega$ , 8k $\Omega$ , 10k $\Omega$ , 14k $\Omega$ , 18k $\Omega$ , 20k $\Omega$ , 24k $\Omega$ , 28k $\Omega$ , 40k $\Omega$ | 1.3     |         | 40      | k $\Omega$ |
| $dR_{TH}, dR_{TL}$     | TOP/BOT bias resistor process variation                              |  | -30     |         | 30      | %          |
| TK of $R_{TH}, R_{TL}$ | TOP/BOT bias resistor temperature variation                          | T = -55 $^{\circ}$ C to 125 $^{\circ}$ C   |         |         | 1.3     | %          |

**Table 3: Analog-to-Digital Converter (ADC)**

| Symbol              | Parameter   | Conditions  | Minimum | Typical | Maximum | Units              |
|---------------------|---|---|---------|---------|---------|--------------------|
| $r_{ADC}$           | Resolution  |   | 10      | 16      | 24      | Bit                |
| $V_{ADCmid}$ (AGND) | Differential ADC input Common Mode                | With internal regulator supplying TOP pin, typical: $V_{TOP/2} = 875mV$ (=PGA output Common Mode level) |         | 0.5     |         | $V_{TOP}$          |
| $\Delta_{ADC,c}$    | Differential input offset shift                   | Sensor signal offset versus maximum sensor signal.<br>Programmable in 8 steps.                          | 0       |         | 7/8     | $V_{shift}/V_{fs}$ |
| ENOB <sup>1</sup>   | Effective number of bits, $3\sigma_{Noise}$ based | Gain = 1.32, $r_{ADC} = 24$ bit, no oversampling  |         | 17      |         | Bit                |
|                     |   | Gain = 28, $r_{ADC} = 16$ bit, no oversampling  |         | 12      |         | Bit                |
|                     |   | Gain = 100, $r_{ADC} = 15$ bit, no oversampling   |         | 10      |         | Bit                |
|                     |   | Gain = 495, $r_{ADC} = 24$ bit, no oversampling   |         | 11      |         | Bit                |

<sup>1</sup>  $ENOB = \text{LOG}_2 \left( \frac{2^{r_{ADC}}}{3\sigma_{Noise}} \right)$  with for example,  $r_{ADC}$  [Bit] = 24.

Table 4: Digital-to-Analog Converter (DAC) and Analog Output

| Symbol                  | Parameter  | Conditions   | Minimum         | Typical | Maximum | Units |
|-------------------------|--|--|-----------------|---------|---------|-------|
| VDD                     | VDD operating range  | AOUT modes using 1V buffer   | 1.8             |         | 5.5     | V     |
|                         |  | AOUT modes using 5V buffer   | 2.7             |         | 5.5     |       |
| t <sub>AOUTsettle</sub> | Time from digital value applied at DAC and voltage at VOUT | 10% to 90% input step:<br>V <sub>AOUT</sub> at 90% of final value                |                 |         | 100     | μs    |
| V <sub>OUT_START</sub>  | Voltage at AOUT during startup                             |  |                 | 0       |         | V     |
| V <sub>AOUT</sub>       | Output voltage at pin AOUT                                 | Ratiometric Voltage Mode   | 0               |         | VDD     | V     |
|                         |  | 1V absolute Voltage Mode   | 0               |         | 1       |       |
| I <sub>OUTMAX</sub>     | Short current limit at pin AOUT                            | AOUT modes using 5V Buffer<br>• short to VDD or VSS<br>• programmable in 4 steps | 3               | 5       | 9       | mA    |
|                         |  |  | 8               | 12      | 20      |       |
|                         |  |  | 15              | 19      | 23      |       |
|                         |  |  | 20              | 25      | 30      |       |
| C <sub>load</sub>       | Load capacitance at AOUT                                   | For example: cap for EMC: 33nF, ECU load: 10nF)                                  | 10 <sup>1</sup> |         | 50      | nF    |
| r <sub>DAC</sub>        | Resolution   |  |                 | 16      |         | Bit   |

<sup>1</sup> In case of enabled Power-Ground Loss detection minimum 10nF on AOUT is required.

Table 5: Programmable-Gain Amplifier (PGA)

| Symbol               | Parameter                       | Conditions   | Minimum | Typical | Maximum | Units            |
|----------------------|---------------------------------|--|---------|---------|---------|------------------|
| G <sub>amp</sub>     | Gain                            | 120 steps  | 1.32    |         | 495     | V/V              |
| G <sub>err</sub>     | Gain error                      | Referenced to nominal gain<br>Gain = 1.32...5                                | -2.5    | 0       | 2.5     | %                |
|                      |                                 | Gain = 6...125   | -5      |         | 5       |                  |
|                      |                                 | Gain = 126...495   | -10     |         | 10      |                  |
| G <sub>errTemp</sub> | Gain error over-temperature     | Temperature compensated sensors do not require calibration over temperature. | -0.2    |         | 0.2     | %                |
| V <sub>CMin</sub>    | Supported input Common Mode     |  | 0.2     | 0.5     | 0.7     | V <sub>TOP</sub> |
| V <sub>ioffsc</sub>  | Differential input offset shift | Programmable in 30 steps:<br>Gain1 ≤ 223                                     | -28.1   | 0       | 28.1    | mV               |
|                      |                                 | Gain1 = 275  | -22.5   | 0       | 22.5    |                  |

Table 6: Sensor Signal Conditioning (SSC) Performance

| Symbol               | Parameter          | Conditions   | Minimum | Typical | Maximum | Units |
|----------------------|--------------------|--|---------|---------|---------|-------|
| OUR                  | Output Update Rate | • 3 measurements: signal+, signal-, diagnosis<br>• r <sub>ADC</sub> = 16bit (main)<br>• r <sub>ADC</sub> = 15bit (temp)<br>• diagnosis ≤ 350μs<br>• SSC-corrected digital output |         | 1.15    |         | kHz   |
|                      |                    | • 2 measurements: signal+, diagnosis<br>• r <sub>ADC</sub> = 15bit (main)<br>• r <sub>ADC</sub> = 15bit (temp)<br>• diagnosis ≤ 350μs<br>• SSC-corrected digital output          |         | 1.82    |         | kHz   |
| t <sub>AOUT_SR</sub> | Step response      | • 3 measurements: signal+, signal-, diagnosis<br>• r <sub>ADC</sub> = 16bit (main)<br>• r <sub>ADC</sub> = 15bit (temp)<br>• diagnosis ≤ 350μs<br>• at AOUT (90% final)          |         | 1.51    |         | ms    |
|                      |                    | • 3 measurements: signal+, signal-, diagnosis<br>• r <sub>ADC</sub> = 15bit (main)<br>• r <sub>ADC</sub> = 15bit (temp)<br>• diagnosis ≤ 350μs<br>• at AOUT (90% final)          |         | 0.86    |         | ms    |

Table 7: Analog Inputs

| Symbol   | Parameter  | Conditions  | Minimum | Typical | Maximum | Units      |
|--|--|---|---------|---------|---------|------------|
| $V_{INP1}$ ,<br>$V_{INN1}$ ,<br>$V_{INP2}$ ,<br>$V_{INN2}$ | Absolute sensor input                            | Voltages at INPx and INNx pin;<br>resulting minimum/maximum differential<br>voltages:<br>$800mV < V_{INDiff} < 800mV$         | 0.2     |         | 1.2     | V          |
| $V_{TEXT}$   | External temperature diode or<br>RTD input range | at T1, T2, T3 pin (see Sensor Supply<br>section of this table and<br>ExtTempBrdgIBias for available<br>configuration options) | 0.3     |         | 1.2     | V          |
| $R_{SENSOR}$   | External sensor (bridge)<br>resistance           | TOP = 1.65V   | 0.825   |         | 60      | k $\Omega$ |
|  |  | 2-wire Current Loop Mode  | 3.3     |         | 60      | k $\Omega$ |
| $ V_{DIFFin} $   | Differential input signal range                  | Referenced to sensor supply ( $V_{DDA_{int}}$ )   |         |         | 800     | mV         |

Table 8: Diagnostics

| Symbol              | Parameter  | Conditions  | Minimum | Typical | Maximum | Units      |
|---------------------|--|---|---------|---------|---------|------------|
| $R_{open}$          | Broken sensor: values $>R_{open}$ set<br>a failure flag                                | • INP1 vs. INN1<br>• INP2 vs. INN2  | 100     | 120     | 150     | k $\Omega$ |
| $R_{short}$         | Shorted sensor: values $<R_{short}$ set<br>a failure flag                              | • INP1 vs. INN1<br>• INP2 vs. INN2<br>• INP1 vs. INP2<br>• INP2 vs. INN1  | 120     |         | 220     | $\Omega$   |
| $I_{leak}$          | Sensor leakage check   | Sensor leakage current from INP/INN to<br>VSS: values $>I_{leak}$ set a failure flag                                    | 0.8     | 1       | 2       | $\mu A$    |
| $V_{common}$        | Sensor Common Mode check<br>(measurement $V_{INP} - V_{AGND}$ , $V_{INN} - V_{AGND}$ ) | Detects sensor connection failure:<br>• open TOP or BOT<br>• short INP or INN to TOP or BOT                             | 0.4     |         | 0.6     | $V_{TOP}$  |
| $V_{drift}$         | AFE gain check, run<br>measurement with dedicated gain,<br>compare with stored values  | Input value from RDAC is applied  |         |         |         |            |
| $V_{RDAC}$          | RDAC differential output voltage   | VDDAx = 1.65V:<br>• S = 00  |         | 2       |         | mV         |
|                     |  | • S = 01  |         | 10      |         |            |
|                     |  | • S = 10  |         | 100     |         |            |
|                     |  | • S = 11  |         | 200     |         |            |
| $R_{T\_OPEN}$       | T1, T2, T3 connection check:<br>open   | Broken Tx sensor: values $>R_{T\_OPEN}$ set<br>a failure flag:<br>• 3 level can be configured<br>• INN is drawn to VSS! | 1.6     | 2       | 3       | M $\Omega$ |
|                     |  |   | 0.4     | 0.5     | 0.6     |            |
|                     |  |   | 0.07    | 0.1     | 0.13    |            |
| $t_{T\_OPEN}$       | Diagnosis time; depends on $C_{ts}$<br>and $R_{T\_OPEN}$                               | Time spent between failure occurrence<br>and output signalization.  | 0.1     |         | 10      | ms         |
| $R_{T\_SHORT}$      | T1, T2, T3 connection check:<br>short to TOP, BOT, INP, INN                            | Shorted Tx sensor: values $<R_{T\_SHORT}$<br>set a failure flag:<br>• configuration for Pt1000                          | 320     | 500     | 650     | $\Omega$   |
| VDD                 | Programmed (expected) VDD<br>level   | Programmable in 6 steps:<br>2.2V, 2.7V, 3V, 4V, 5V, 5.25V   | 2.2     |         | 5.25    | V          |
| VDDD <sub>BOD</sub> | VDDD brown out detection   | VDDD < VDDD <sub>BOD</sub> system is in reset<br>state  | 85      |         | 92      | %VDDD      |
| $V_{LOSS}$          | Power/ground loss with respect to<br>AOUT  | • VAOUT – VDD > $V_{LOSS}$<br>• VAOUT – VSS < $V_{LOSS}$  |         | 0.2     |         | V          |

Table 9: Power-Up

| Symbol     | Parameter    | Conditions  | Minimum | Typical | Maximum | Units   |
|------------|--------------|---|---------|---------|---------|---------|
| $t_{STA1}$ | Startup time | VDD ramp up to interface<br>communication                             |         |         | 10      | ms      |
| $t_{STA2}$ |              | VDD ramp up to analog operation;<br>depends on the configuration used |         |         | 10      | ms      |
| $t_{WUP1}$ | Wake-up time | Sleep to Active State interface<br>communication                      |         | 2       | 10      | $\mu s$ |



Table 10: Oscillator

| Symbol              | Parameter                        | Conditions               | Minimum | Typical | Maximum | Units |
|---------------------|----------------------------------|--------------------------|---------|---------|---------|-------|
| f <sub>CLK_HF</sub> | Internal HF-oscillator frequency | At T=27°C                | 15.8    | 16      | 16.2    | MHz   |
|                     |                                  | Across temperature range | 15.4    |         | 16.6    |       |
| f <sub>CLK_LF</sub> | Internal LF-oscillator frequency |                          | 25      | 32      | 41      | kHz   |

Table 11: Internal Temperature Sensor

| Symbol            | Parameter                              | Conditions                  | Minimum | Typical | Maximum | Units |
|-------------------|--|-----------------------------|---------|---------|---------|-------|
| Γ <sub>Temp</sub> | Internal temperature sensor resolution | Differential output voltage |         | 220     |         | μV/K  |

Table 12: Digital IO Pins

| Symbol                | Parameter                            | Conditions  | Minimum | Typical | Maximum | Units |
|-----------------------|--------------------------------------|---|---------|---------|---------|-------|
| V <sub>IL</sub>       | Input low Voltage                    | voltage level where the input is recognized as low level  |         |         | 30      | % VDD |
| V <sub>IH</sub>       | Input high Voltage                   | voltage level where the input is recognized as high level | 70      |         |         | % VDD |
| V <sub>Ihys</sub>     | Input hysteresis                     |   | 10      |         | 35      | % VDD |
| V <sub>OL</sub>       | Output low Voltage                   |   |         |         | 8       | % VDD |
| V <sub>OH</sub>       | Output high Voltage                  |   | 92      |         |         | % VDD |
| I <sub>OL</sub>       | Output drive low current             | V <sub>PAD</sub> = V <sub>OL</sub>                        | 1       |         | 2.4     | mA    |
|                       |                                      | VDD = 1.7V  |         |         | 6.6     |       |
|                       |                                      | VDD = 2.6V  |         |         | 20      |       |
|                       |                                      | VDD = 5V  |         |         | 9       |       |
| I <sub>OH</sub>       | Output drive high current            | V <sub>PAD</sub> = V <sub>OH</sub>                        | 1.2     |         | 2.3     | mA    |
|                       |                                      | VDD = 1.7V  |         |         | 6.4     |       |
|                       |                                      | VDD = 2.6V  |         |         | 20.2    |       |
|                       |                                      | VDD = 5V  |         |         | 10.9    |       |
| I <sub>pullup</sub>   | Weak pull-up current at pin RESN     | V <sub>PAD</sub> = 0V                                     | 5       |         | 13      | μA    |
|                       |                                      | VDD = 1.7V  |         |         | 50      |       |
|                       |                                      | VDD = 2.6V  |         |         | 84      |       |
|                       |                                      | VDD = 5V  |         |         | 250     |       |
| I <sub>pulldown</sub> | Weak pull-down current at pin WAKEUP | V <sub>PAD</sub> = VDD                                    | 5       |         | 11      | μA    |
|                       |                                      | VDD = 1.7V  |         |         | 35      |       |
|                       |                                      | VDD = 2.6V  |         |         | 80      |       |
|                       |                                      | VDD = 5V  |         |         | 160     |       |

Table 13: Serial Interfaces

| Symbol              | Parameter                                   | Conditions | Minimum | Typical | Maximum | Units  |
|---------------------|---|------------|---------|---------|---------|--------|
| f <sub>C,UART</sub> | UART clock frequency (for IO-Link protocol) |            |         | 230.4   |         | kBit/s |
| f <sub>C,I2C</sub>  | I2C clock frequency                         |            |         |         | 1       | MHz    |
| CD <sub>OWI</sub>   | OWI data rate                               |            |         | 4       |         | kBit/s |

Table 14: Flash Memory

| Symbol               | Parameter        | Conditions   | Minimum | Typical | Maximum | Units   |
|----------------------|------------------|--|---------|---------|---------|---------|
| t <sub>PROG</sub>    | NVM program time | Programming time for complete configuration and calibration page |         | 360     |         | ms      |
| η <sub>NVM</sub>     | NVM endurance    | Number of reprogramming cycles                                   | 20000   |         |         | Numeric |
| t <sub>RET,NVM</sub> | Data retention   |  | 10      |         |         | Years   |

### 3 Basic System Configuration

#### 3.1 System Modes/System Start

The ZSSC3286 can operate in three different main operating modes:

- Bootloader** It is started after successfully passing the initialization phase of the ZSSC3286 hardware. ZSSC3286 checks that firmware and CCP CRC are correct to allow starting the firmware in SIO Mode. The bootloader allows to update the CCP content.
- Standard I/O Mode (SIO)** It is the startup operation mode after passing the bootloader. The SIO mode supports the Command Mode and Cyclic Mode operational states. ZSSC3286 waits for actions on I2C interface or the wakeup request (WURQ) to start transition to IO-Link COM Mode.
- I/O-Link COM Mode** It is the default operation mode if IO-Link communication is established during operation in the field or during calibration process. The I/O Link COM mode supports the Command Mode and Cyclic Mode operational states.

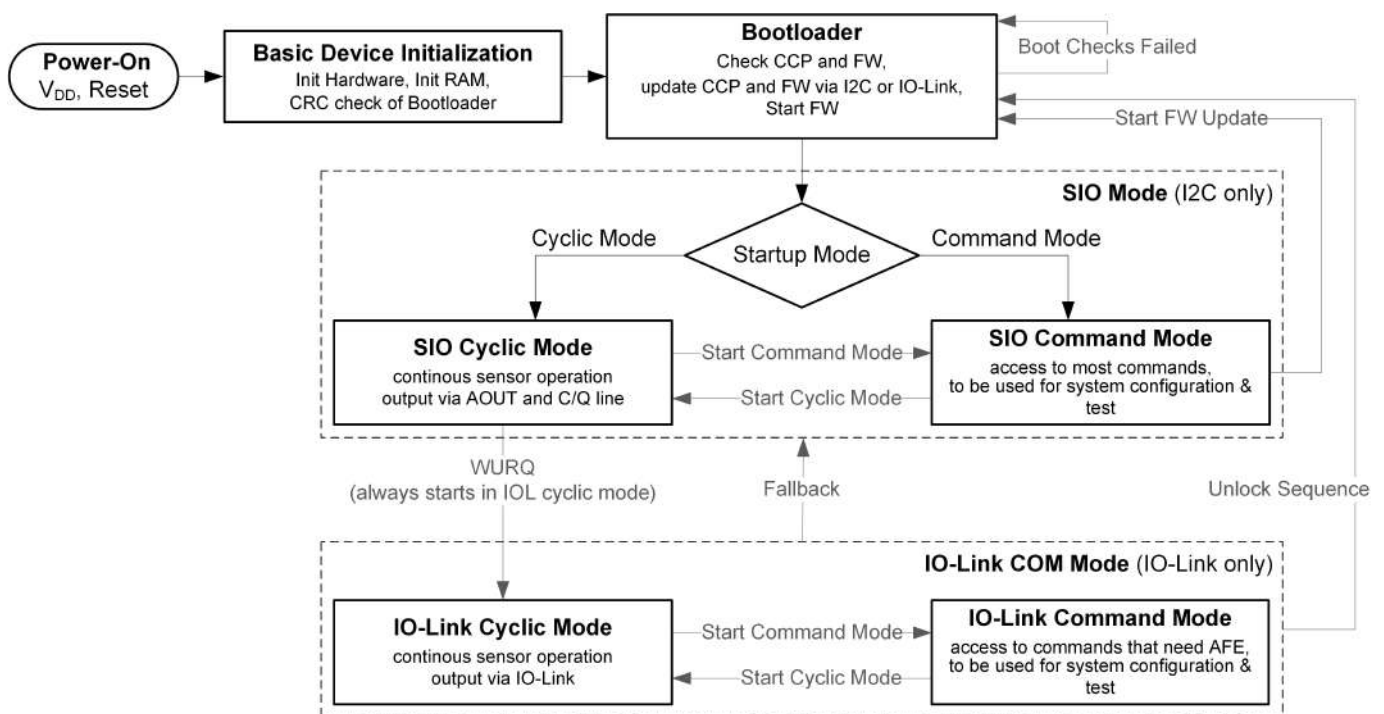


Figure 5: Main Operation Modes

SIO Mode and I/O-Link Mode will support the following operation states:

- Cyclic Mode** This is the default mode for continuously operating sensors. In this mode autonomous, cyclically repeated sensor measurements are performed and related digital (via IO-Link in IO-Link COM Mode), and/or analog output (via AOUT in SIO Mode) and/or digital alarm output (C/Q line in SIO Mode) updates are provided. The cyclic sequences for sensor measurements and system diagnostic measurements are configurable and allow to define the output update rate of the conditioned sensor signals.
- Command Mode** This is the most appropriate mode for evaluation, test, and calibration purposes. In this mode, all commands to support calibration process via serial interface commands are available. Command Mode can be used for applications requiring re-occurring digital interaction on functions that are not available in Cyclic Mode or certain system configuration changes.



## 4 Analog Front End (AFE)

### 4.1 AFE Signal Path

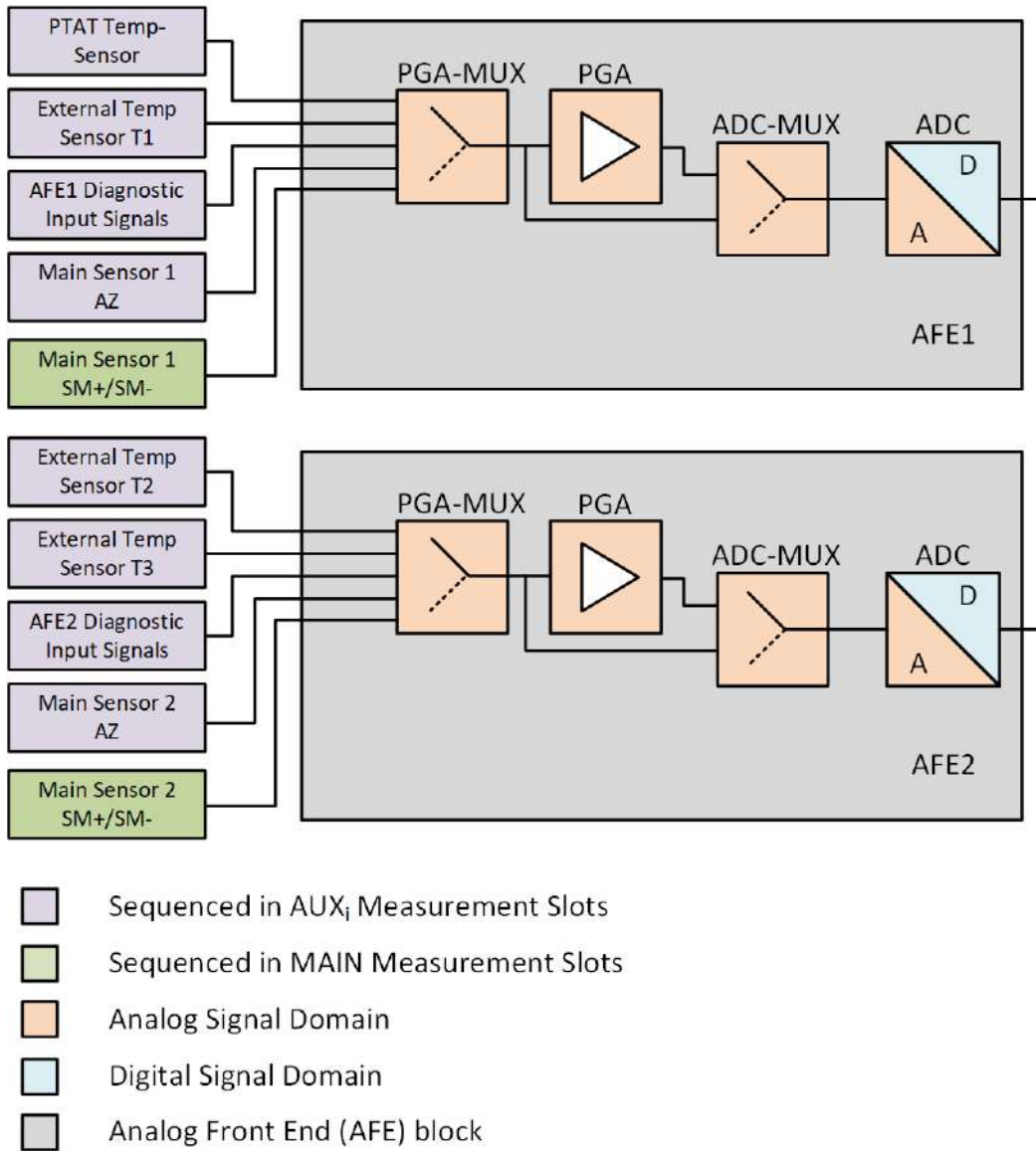


Figure 6: Block Diagram Analog Front End

## 4.2 Bridge Sensor Inputs

### 4.2.1 Resistive Bridge Sensors

Table 16: Resistive Bridge Parameters

| Symbol    | Parameter   | Conditions  | Minimum | Typical | Maximum | Units           |
|-----------|---|---|---------|---------|---------|-----------------|
| $R_{br}$  | Bridge resistor   | Constant Voltage Mode   | 0.825   |         | 60      | k $\Omega$      |
|           |   | Constant Current Mode   | 0.1     |         |         |                 |
| $C_{br}$  | Bridge capacitance, depends on the required resolution:<br>$\tau = R_{br} \times C_{br}$ defines the settle time. | Filter capacitances $C_{br}$ between INN $x$ /INP $x$ and VSS         |         | 1       |         | nF              |
| $V_{sig}$ | Signal span   | mV/V is related to the bridge supply                                  |         |         | 500     | mV/V            |
| $V_{off}$ | Signal offset   | For example:<br>$V_{sig} = 1\text{mV}$ allows $V_{off} = 20\text{mV}$ |         |         | 2000    | % off $V_{sig}$ |
|           |   |   |         |         | 20      | $1/V_{sig}$     |

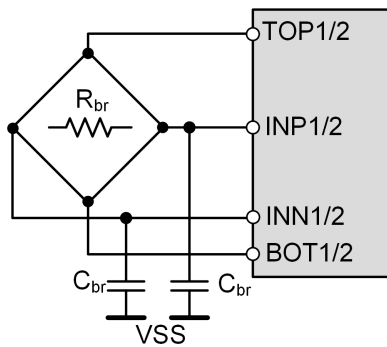


Figure 7: Bridge Sensor Type 1

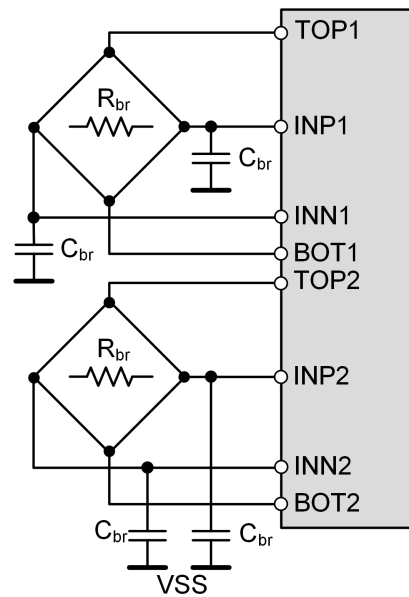
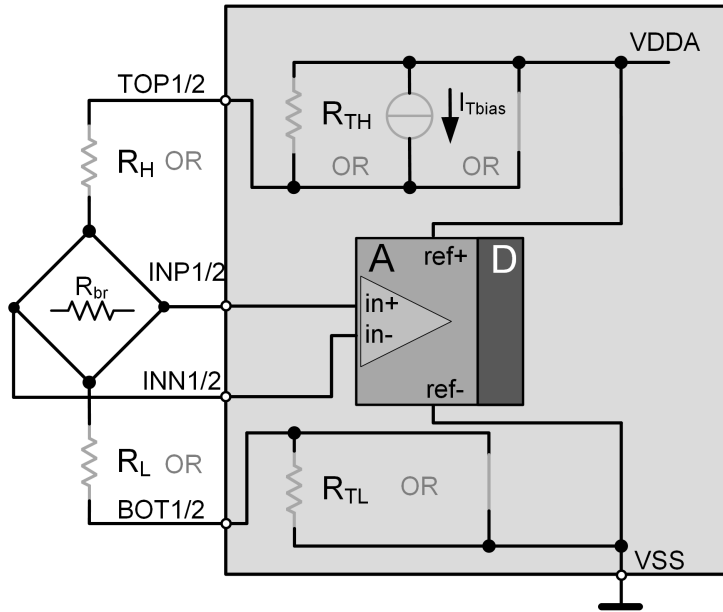


Figure 8: Bridge Sensor Type 2

In single bridge applications shown in Figure 7 the resistive bridge can be connected to either AFE1 or AFE2 depending on PCB layout requirements.

The resistive bridge can be sourced in either Constant Voltage mode (V-source) or in Constant Current mode (I-source), whereby last mode requires low bridge resistance.



Legend:

Gray components: can be activated “either-or” via the GUI.

**Figure 9: Resistive Bridge Bias Configurations**

In Constant Current mode the bridge output must be set within the common input range of the PGA. This can be done with a low side external resistor  $R_L$  or with the internal resistor  $R_{TL}$ . The current that is supplied to the bridge must be adjusted to bridge resistance and this additional  $R_L$  or internal  $R_{TL}$  to meet the common input range of PGA. In Constant Voltage mode the bridge current can be reduced by inserting the internal high and low side resistors  $R_{TH}$ ,  $R_{TL}$  or by adding external resistors  $R_H$  and  $R_L$ .

**Table 17: Resistive Bridge Supply Parameters**

| Symbol           | Parameter                | Conditions   | Minimum | Typical | Maximum | Units      |
|------------------|--------------------------|--|---------|---------|---------|------------|
| $V_{TOP1/2}$     | Output voltage at TOP1/2 |  |         | VDDA    |         | V          |
| $I_{load}$       | Load current             | In Constant Voltage mode defined by bridge resistance      |         |         | 2       | mA         |
| $I_{Rbr\_bias}$  | Current out of TOP1/2    | In Constant Current mode adjustable via <i>BmBrdgIBias</i> | 5       |         | 500     | $\mu$ A    |
| $C_{TOP\_BOT}$   | Load capacitance         |  |         |         | 2.2     | nF         |
| $R_{TH}, R_{TL}$ | Bias resistor            |  | 1.3     |         | 40      | k $\Omega$ |

## 4.3 Auxiliary Temperature Sensor Inputs

### 4.3.1 Internal PTAT Temperature Sensor

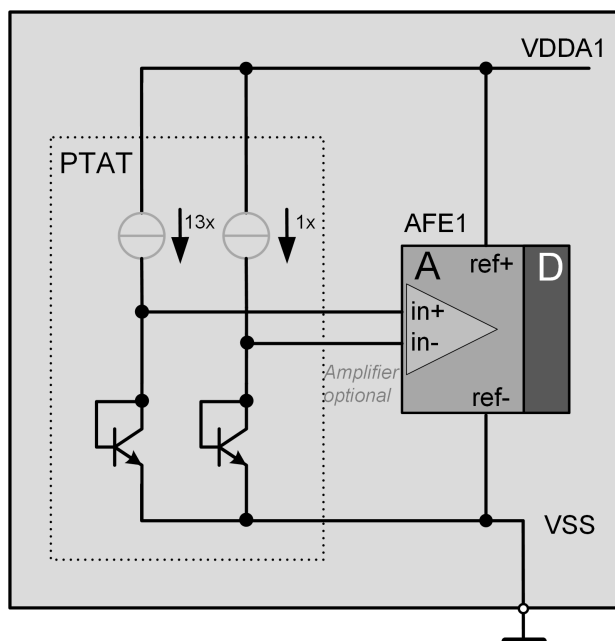


Figure 10: PTAT Sensor Configuration

Table 18: Internal PTAT Parameters

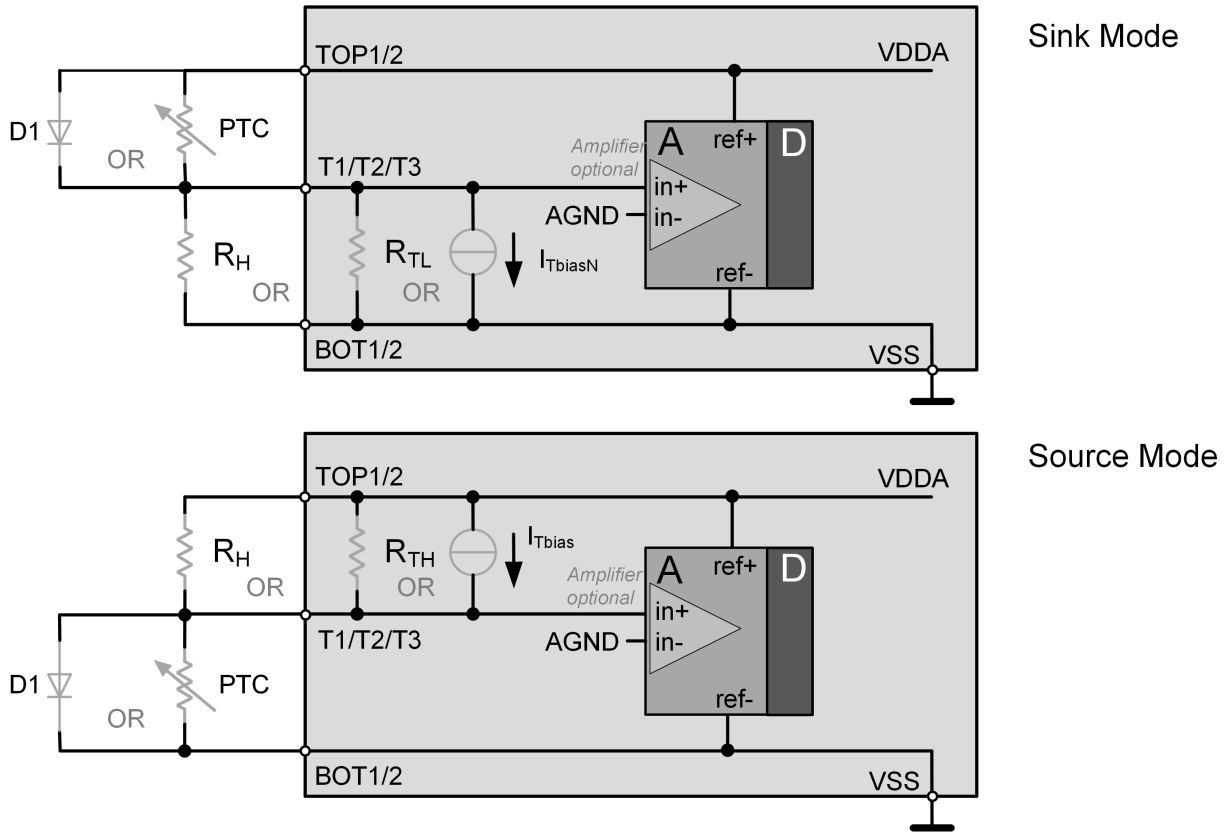
| Symbol             | Parameter            | Conditions                  | Minimum | Typical | Maximum | Units           |
|--------------------|----------------------|-----------------------------|---------|---------|---------|-----------------|
| $T_{\text{meas}}$  | Measurement range    |                             | -55     |         | 125     | °C              |
| $E_T$              | Measurement error    | Calibrated                  | -5      |         | 5       | K               |
| $ADC_{\text{res}}$ | Resolution           | Programmable ADC resolution | 10      |         | 15      | bit             |
| $T_{\text{res}}$   | Effective resolution | $\pm 1.5\sigma$             | 2       |         |         | LSB/°C          |
| S                  | Sensitivity          | Differential output voltage | 218     |         | 230     | $\mu\text{V/K}$ |

### 4.3.2 External Temperature Sensors

Three different external sensor types can be used to measure the temperature of the main sensor or a media temperature in the auxiliary signal path of the AFEs:

- PTC
- Diode
- TC Bridge Sensor

The PTC and Diode Sensors can be supplied either in Sink Mode or in Source Mode as shown in Figure 11. The gray marked components can be activated “either-or” via the GUI. The AGND potential is at  $VDDA/2$ .



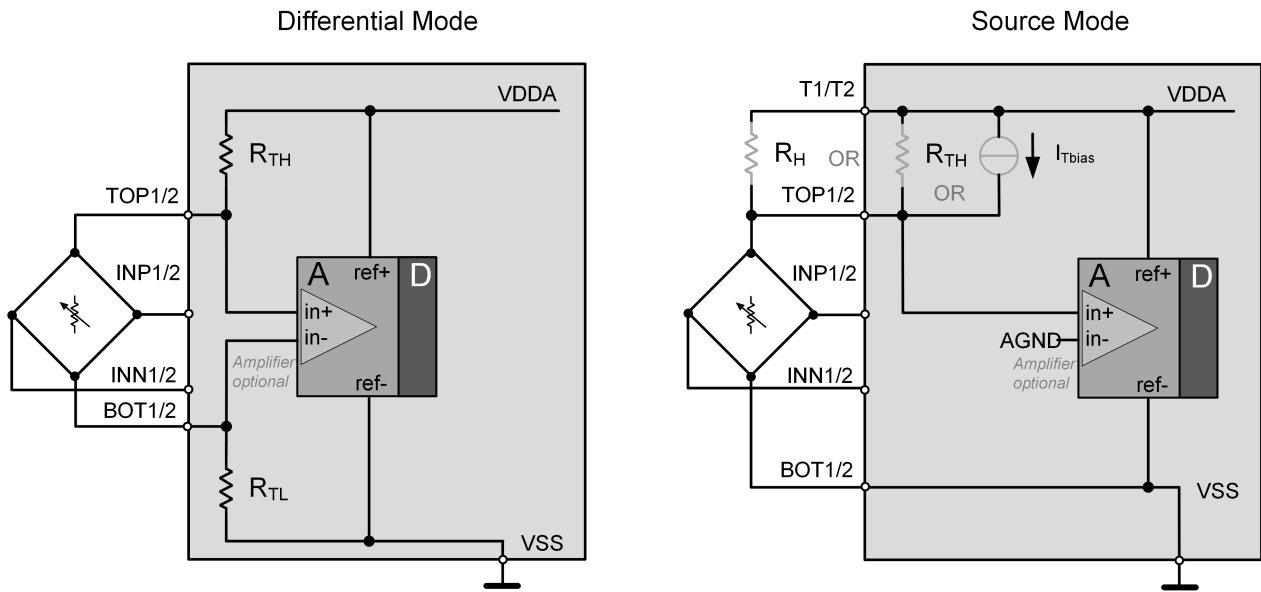
Legend:

Gray components: can be activated “either-or” via the GUI. The AGND potential is at  $VDDA/2$ .

**Figure 11: PTC, Diode Sensor Bias Configurations**



TC Bridge Sensor configurations can be supplied in Differential Mode or Source Mode as shown in Figure 12.



Legend:

Gray components: can be activated “either-or” via the GUI. The AGND potential is at VDDA/2.

Figure 12: TC Bridge Sensor Bias Configurations

Table 19: External Temperature Sensor Parameters

| Symbol              | Parameter                                | Conditions                  | Minimum | Typical | Maximum | Units    |
|---------------------|--|-----------------------------|---------|---------|---------|----------|
| $R_{\text{sensor}}$ | Sensor resistance (PTC/TC Bridge Sensor) |                             | 50      |         | 1M      | $\Omega$ |
| $ADC_{\text{res}}$  | ADC resolution                           | Programmable ADC resolution | 10      |         | 15      | bit      |
| ENOB                | Effective resolution                     | $\pm 1.5\sigma$             | 14      |         |         | bit      |

#### 4.4 Programmable Gain Amplifier (PGA)

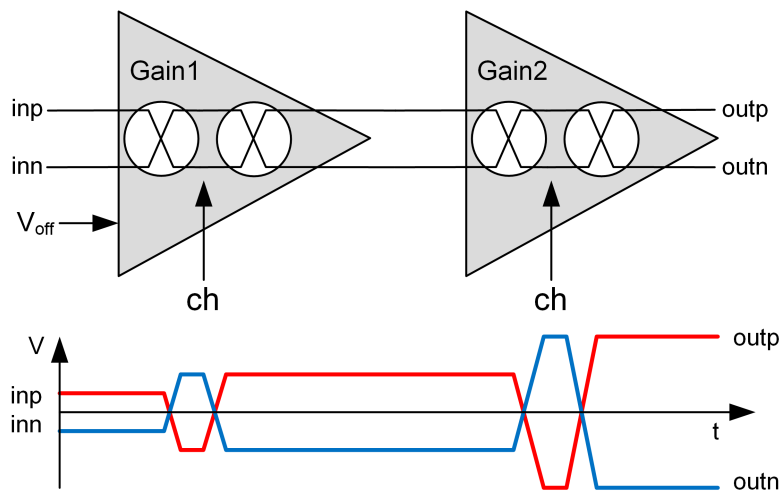


Figure 13: PGA Architecture

The first amplifier (Gain1) has a built in PGA offset compensation (auto-zero) that is refreshed at the beginning of every measurement. The second stage has no offset compensation. The second stage amplifier offset is present at the PGA output with offset  $\times$  Gain2. Both PGA amplifier stages have built-in chopper functionality to suppress 1/f noise.

The gain settings that can be selectively programmed for both PGA stages are listed in Table 20.

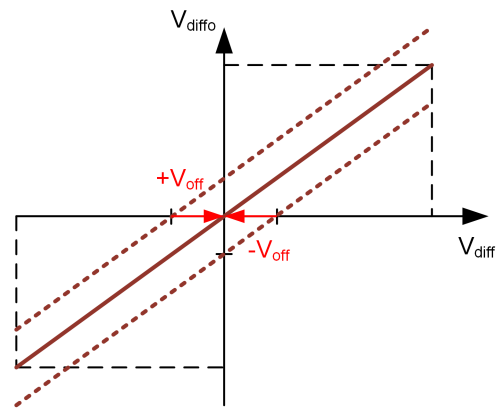
**Table 20: PGA Gain Steps**

| Gain1 | Gain2 |
|-------|-------|
| 1.2   | 1.1   |
| 2     | 1.2   |
| 4     | 1.3   |
| 5.97  | 1.4   |
| 11.9  | 1.5   |
| 19.8  | 1.6   |
| 29.6  | 1.7   |
| 39.2  | 1.8   |
| 58.1  |       |
| 76.6  |       |
| 112   |       |
| 143   |       |
| 187   |       |
| 223   |       |
| 275   |       |

If bridge sensors show noticeable DC offsets in their differential output voltage (usable differential voltage range is offset from zero) this limits the maximum PGA gain, which can be applied without putting the PGA into saturation. To compensate for such sensor offsets, the PGA can be programmed to shift the input signal by an offset voltage shown in Table 21 and Figure 14 before it gets gained up. The default shift is 0mV, the offset can be compensated by 15 steps in positive and negative direction as shown in Table 21. The PGA offset shift function is offered only for PGA Gain1 ≥ 11.9.

**Table 21: PGA Input Offset Compensation Steps**

| 11.9 ≤ Gain1 ≤ 223 [mV] | Gain1 = 275 [mV] |
|-------------------------|------------------|
| 0                       | 0                |
| ±1.9                    | ±1.5             |
| ±3.8                    | ±3               |
| ±5.6                    | ±4.5             |
| ±7.5                    | ±6               |
| ±9.4                    | ±7.5             |
| ±11.3                   | ±9               |
| ±13.1                   | ±10.5            |
| ±15                     | ±12              |
| ±16.9                   | ±13.5            |
| ±18.8                   | ±15              |
| ±20.6                   | ±16.5            |
| ±22.5                   | ±18              |
| ±24.4                   | ±19.5            |
| ±26.3                   | ±21              |
| ±28.1                   | ±22.5            |



**Figure 14: PGA Input Offset Compensation**

PGA gain and the Input Offset Compensation value can be programmed separately for the two main bridge sensors and for the three external auxiliary temperature sensors that can be connected to the ZSSC3286. The PGA Input Offset Compensation feature is limited to SM+/SM- and SM+ sequencer configurations which are described in subsection 4.6.

Table 22: PGA Parameters

| Symbol              | Parameter                 | Conditions   | Minimum | Typical | Maximum | Units |
|---------------------|---------------------------|--|---------|---------|---------|-------|
| Gain                | Total PGA gain            | Programmable in 15/8 steps:<br>• stage1: 15 steps, 1.2 to 275<br>• stage2: 8 steps, 1.1 to 1.8 | 1.32    |         | 495     | V/V   |
| V <sub>cmi</sub>    | Input Common Mode voltage |  |         | VDDA/2  |         | V     |
| BW <sub>PGA</sub>   | Bandwidth                 |  |         | 5       |         | kHz   |
| t <sub>az_PGA</sub> | Auto-zero time            |  | 10      |         |         | μs    |
| f <sub>ch_PGA</sub> | Chopper frequency         |  |         | 100     |         | kHz   |

## 4.5 Analog-to-Digital Converter (ADC)

An incremental delta-sigma analog-to-digital converter (ADC) is used to digitize the PGA signal. To allow optimizing the trade-off between conversion time and resolution, the resolution can be programmed from 10-bit to 24-bit. The ADC processes differential input signals around its input Common Mode level VDDA/2. Table 23 lists the ADC resolution, signal ranges, conversion times for a single analog-to-digital conversion and VDDA = 1.65V.

Table 23: ADC Configuration Parameters

| ADC Resolution [Bits] | Full Scale Input Voltage V <sub>fs</sub> [V] | LSB Size V <sub>LSB</sub> [μV] | Conversion Time, Typical, T <sub>Conv</sub> [μs] | Conversion Rate, Typical, F <sub>Conv</sub> [kHz] |
|-----------------------|--|--------------------------------|--|---|
| 10                    | ±1.418                                       | 2768.638                       | 32.54  | 30.73   |
| 11                    | ±1.425                                       | 1391.718                       | 43.75  | 22.86   |
| 12                    | ±1.431                                       | 698.499                        | 59.59  | 16.78   |
| 13                    | ±1.434                                       | 350.189                        | 81.99  | 12.20   |
| 14                    | ±1.437                                       | 175.428                        | 113.68   | 8.80  |
| 15                    | ±1.439                                       | 87.832                         | 158.49   | 6.31  |
| 16                    | ±1.440                                       | 43.958                         | 221.86   | 4.51  |
| 17                    | ±1.441                                       | 21.994                         | 311.48   | 3.21  |
| 18                    | ±1.442                                       | 11.002                         | 438.22   | 2.28  |
| 19                    | ±1.443                                       | 5.503                          | 617.46   | 1.62  |
| 20                    | ±1.443                                       | 2.752                          | 870.94   | 1.15  |
| 21                    | ±1.443                                       | 1.376                          | 1229.41  | 0.81  |
| 22                    | ±1.443                                       | 0.688                          | 1736.38  | 0.58  |
| 23                    | ±1.443                                       | 0.344                          | 2453.33  | 0.41  |
| 24                    | ±1.444                                       | 0.172                          | 3467.25  | 0.29  |

The ADC can perform an additional offset shift (independent of the PGA shifting) to adapt input signals with offsets to the ADC input range. Enabling the offset shift causes the ADC to perform an additional amplification of the ADC's input signal by factor ×2. This must be considered for a correct PGA configuration setup.

The ADC offset shift feature is limited to SM+/SM- and SM+ sequencer configurations which are described in subsection 4.6.

The shift values in Table 24 are related to the input voltages at INP, INN:

- Full scale differential input voltage:  $V_{INdiff\_fs} = \frac{V_{fs}}{Gain}$
- Differential input shift voltage:  $V_{INdiff\_shift}$
- Maximum, minimum differential input voltage:  $V_{INdiff\_max}, V_{INdiff\_min}$

**Table 24: ADC Input Offset Shift Steps**

| PGA Polarity | ADC Shift Enable | ADC Gain | ADC Shift | $V_{INDIFF\_SHIFT} / V_{INDIFF\_FS}$ | $V_{INDIFF\_MIN} / V_{INDIFF\_FS}$ | $V_{INDIFF\_MAX} / V_{INDIFF\_FS}$ |
|--------------|------------------|----------|-----------|--------------------------------------|------------------------------------|------------------------------------|
| Positive     | 0                | x1       | 0         | No shift                             | -1                                 | +1                                 |
| Negative     |                  |          | 0         | No shift                             | +1                                 | -1                                 |
| Positive     | 1                | x2       | 1         | 7/8                                  | -1/16                              | +15/16                             |
|              |                  |          | 2         | 6/8                                  | -2/16                              | +14/16                             |
|              |                  |          | 3         | 5/8                                  | -3/16                              | +13/16                             |
|              |                  |          | 4         | 4/8                                  | -4/16                              | +12/16                             |
|              |                  |          | 5         | 3/8                                  | -5/16                              | +11/16                             |
|              |                  |          | 6         | 2/8                                  | -6/16                              | +10/16                             |
|              |                  |          | 7         | 1/8                                  | -7/16                              | +9/16                              |
| Negative     |                  |          | 0         | No shift                             | -1/2                               | +1/2                               |
|              |                  |          | 0         | No shift                             | +1/2                               | -1/2                               |
|              |                  |          | 1         | 1/8                                  | -9/16                              | +7/16                              |
|              |                  |          | 2         | 2/8                                  | -10/16                             | +6/16                              |
|              |                  |          | 3         | 3/8                                  | -11/16                             | +5/16                              |
|              |                  |          | 4         | 4/8                                  | -12/16                             | +4/16                              |
|              |                  |          | 5         | 5/8                                  | -13/16                             | +3/16                              |
| 6            | 6/8              | -14/16   | +2/16     |                                      |                                    |                                    |
| 7            | 7/8              | -15/16   | +1/16     |                                      |                                    |                                    |

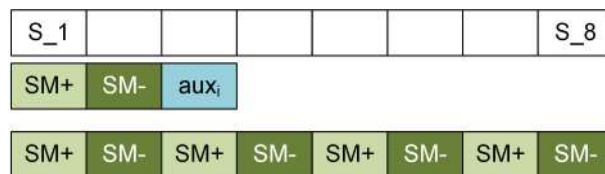
### 4.6 AFE Sequencer

The measurement flow, especially the frequency of main bridge measurements vs. auxiliary measurements can be configured by the user. Once started by the ARM MCU, the measurement flow runs autonomously controlled by the AFE. The AFE Sequencer state machine ensures predictable measurement timing in the continuous cyclic operation of ZSSC3286.

The AFE sequencer carries out AFE measurements based on a measurement slot mechanism. There can be up to eight measurement slots assigned per AFE, which form a single measurement cycle. A measurement cycle can be executed only once (for example, initiated by a dedicated command request) or continuously cycled in Cyclic Mode operation of ZSSC3286.

Each of the measurement slots inside AFE1 or AFE2 can be individually configured for the following measurement types:

- Sensor Measurement (SM+): bridge inputs INP/INN directly converted (non-inverted)
- Sensor Measurement (SM-): bridge inputs INP/INN flipped (inverted)
- Auxiliary Measurement (aux): cycles through the auxiliary measurement vector

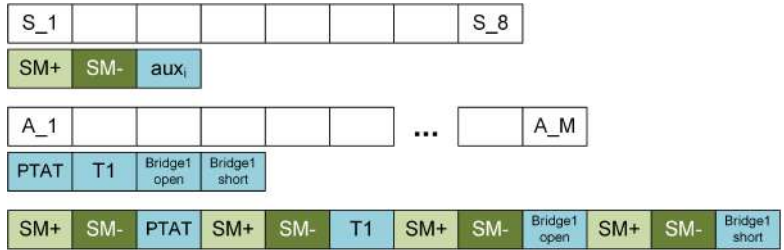


**Figure 15: Measurement Slot Configuration with Two Example Configurations**

The actual number of measurement slots per measurement cycle can be defined by the user between 1 and 8. The hardware allows to configure any combination, but not all combinations lead to reasonable measurement schemes. The GUI supports the user in selecting proper measurement schemes. Figure 15 shows two example configurations. The measurement schemes are explained in further detail in subsection 4.6.3, 4.6.4, and 4.6.5.

Auxiliary measurements usually have lower response time requirements than measurements on the main sensor bridge. The auxiliary measurements are therefore cycled orthogonal to the main loop of the sequencer. Activated

auxiliary measurements become listed in the so called auxiliary measurement vector. The vector index 'i' gets increased after each executed aux<sub>i</sub> slot and starts over after the entire set of active measurements was completed. The configuration options of auxiliary measurements are further detailed in subsection 4.6.2.



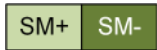
**Figure 16: Auxiliary Measurement Configuration, and Corresponding Measurement Flow**

Figure 16 illustrates the sequencer operation with an example configuration using 4 auxiliary measurements. During the 3rd measurement (configured as aux<sub>i</sub>), the first enabled auxiliary measurement is executed ("PTAT", internal temperature sensor). After the measurement sequence (SM+/SM-/aux<sub>i</sub>) is executed again in the next measurement slot, the next enabled auxiliary measurement is executed ("T1", external temperature sensor). Similarly, "Bridge1 open" and "Bridge1 short" diagnostics measurements are carried out in following measurement slots. During the 5th execution of the measurement sequence, the PTAT auxiliary measurement is carried out again.

**4.6.1 Bridge Sensor Measurement Configuration**

The main bridge sensor signals can be measured in three ways:

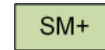
- SM+/SM- (or SM-/SM+) measurement
- SM+/AZ measurement (SM+ and auto-zero measurement)
- SM+ without AUX\_AZ measurement



**Figure 17: SM+/SM- (or SM-/SM+) Measurement**



**Figure 18: SM+/AZ Measurement**



**Figure 19: SM+ without AZ Measurement**

Configurations in Figure 17 and Figure 18 provide digital offset compensation of the entire signal path in the analog front end. The configuration in Figure 19 only provides analog offset compensation in the first stage of the PGA. The offsets of the second PGA stage and the ADC offset are not compensated.

In the SM+/SM- configuration, the bridge inputs INP/INN are first converted straight forward in the SM+ measurement slot and second with an internally flipped INP/INN input signal in SM- slot. For the SM+/AZ configuration, the second measurement (AZ) is performed without applied input signal. INP/INN become disconnected from the sensor and internally shorted for AZ measurements.

Since signal integration time in SM+/SM- configuration is twice as long as in in the SM+/AZ configuration (same ADC resolution settings assumed), the SM+/SM- configuration achieves approx. 0.5 bit better noise performance than the SM+/AZ configuration. The longer input signal integration time of the SM+/SM- configuration leads to an increased output update rate and step response as described in subsection 4.6.3 and subsection 4.6.4.

The auto-zero measurement (AZ) belongs to the group of auxiliary measurements and is cycled less often if either of the following options appears:

- further auxiliary measurements are enabled in the auxiliary measurement vector described in subsection 4.6.2
- accelerated bridge measurements are enabled as described in subsection 4.6.5

Since the offset in the internal signal path varies rather slowly, the auto-zero compensation remains very accurate even for a long auxiliary measurement vector.

Because SM- needs to be configured and most sensor applications also require other auxiliary measurements, the assignment of the AZ measurement to the group of auxiliary measurements helps to reduce the worst case step response on the main bridge sensor.

The lowest step response is achieved with the “SM+ only” configuration shown in Figure 19 if no other auxiliary measurements are needed for the desired sensor application.

A further influence on the overall measurement time (output update rate and worst case response) has the input settling time of each measurement task. This settling is required depending on the output resistance of the external sensors, respective capacitive loads on the signal lines and the ADC resolution selected by the user. The input settling time is always inserted before an ADC conversion starts and can be configured in the GUI for main bridge measurements via Configure/AFE/Bridge/SetTime [μs] and for auxiliary temperature measurements via Configure/AFE/Temperature/SetTime [μs].

Considering achievable measurement latencies and noise performance, configuration shown in Figure 17 is better when higher ADC resolutions are required or for sensor configurations with fast input settling, while configuration shown in Figure 18 and Figure 19 are preferable when lower ADC resolutions become selected or for sensor configurations requiring long input settling times (bridge settling time has a considerable impact on the timing budget).

#### 4.6.2 Auxiliary Measurement Configuration

The supported auxiliary measurements are:

- Auto-zero for internal signal path
- Temperature on sensor input T1
- Temperature on sensor input T2
- Temperature on sensor input T3
- Internal PTAT
- AFE diagnostic checks
  - Sensor connection checks for all external sensors (Short to TOPx pin or BOTx pin and Open)
  - Bridge signal range check
  - AFE gain and offset drift supervision via internal reference DAC

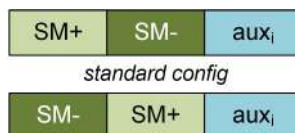
They can be activated in the GUI via tabs Configure/AFE/Sequencer, Configure/AFE/Temperature Selection and Diagnostic/Sensor/AFE.

#### 4.6.3 Timings with SM+/SM- Configuration

As described in subsection 4.6.1, sensor configurations with fast input settling or applications requiring higher ADC resolutions are better served with the SM+/SM- scheme for the main bridge measurement. For the step response consideration the following application example is used:

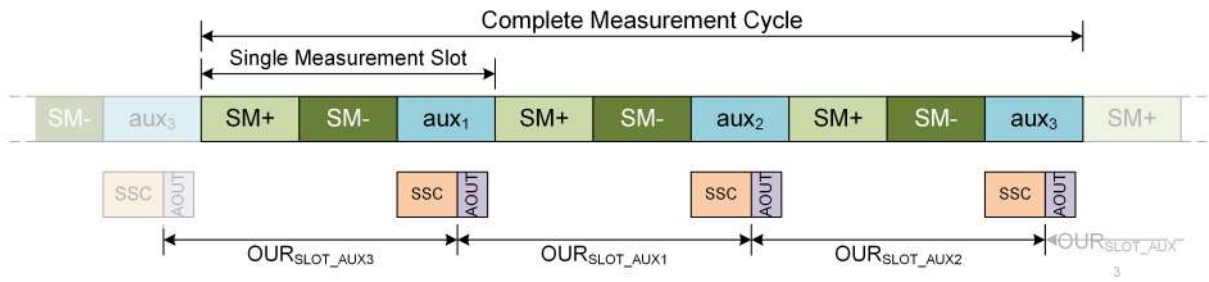
- Sensor Measurement (non-inverted)
- Sensor Measurement (inverted)
- Auxiliary Measurement (for example, for sensor temperature)

**Note:** SM+ and SM- can be exchanged yielding to the same result



**Figure 20: SM+/SM- Configuration**

For SM+/SM- configuration the measurement cycle and output update rate is shown in Figure 21 for an example of three enabled auxiliary measurement tasks. After finishing the last main measurement task, firmware starts with data processing as described in section 5 and section 6. The resulting signal conditioning output signal is written into output registers.



**Figure 21: SM+/SM- Measurement Cycle and Output Update Rate**

For SM+/SM- configuration the worst-case step response is shown in Figure 22 and consists of:

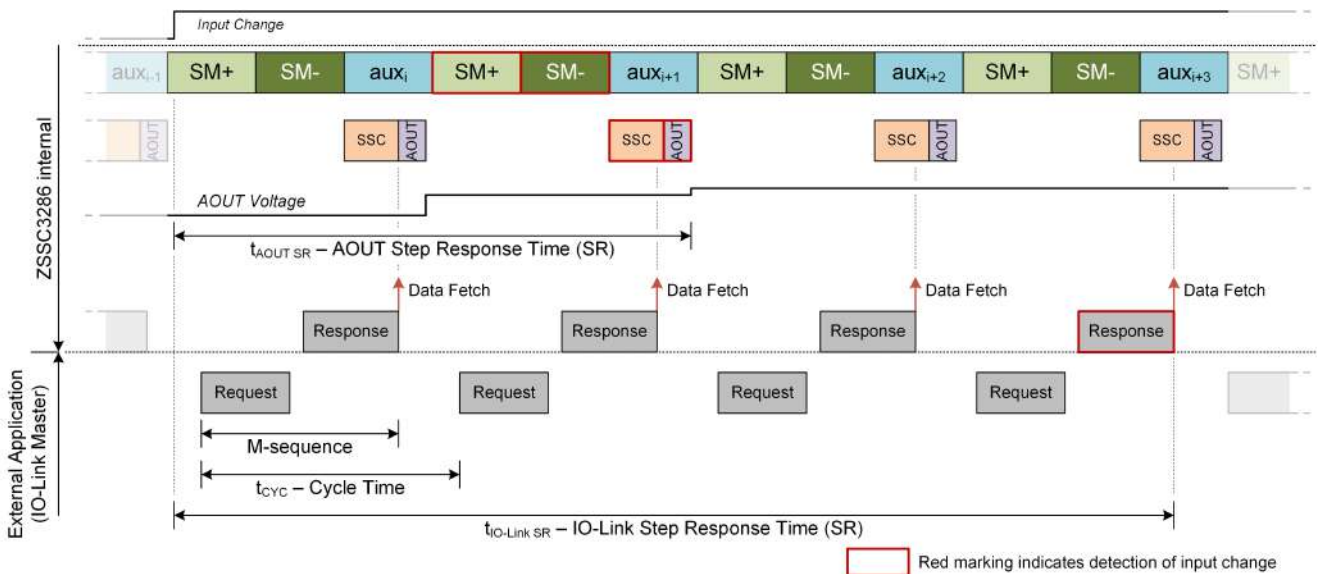
- 4 sensor ADC-conversion times (duration depending on selected ADC resolution)
- 1 auxiliary conversion time (fixed duration, based on longest auxiliary conversion timing)
- 1 SSC calculation

Additionally there is an delay that depends on the selected interface:

- 1 settling time at AOUT for all analog output options
- 2 cycle times for IO-Link communication

Within the worst-case scenario, consider that intermediate results can occur since input changes as well as data readout will be asynchron to the internal running measurement cycle.

Worst-case scenario for IO-Link communication depends on IO-Link master since it defines the cycle time. ZSSC3286 defines minimum cycle time of 600µs.



**Figure 22: SM+/SM- Step Response**

#### 4.6.4 Deterministic Input Step Response with SM+/AZ Configuration

Since the SM+/SM- configuration samples the input signal twice as long as the SM+/AZ configuration and it suffers a noticeable timing overhead for sensor configurations with slow sensor input signal settling, a second SM+/AZ measurement scheme with deterministic step response times is available. For the step response consideration, the following application example is used:

- Sensor measurement (non-inverted)
- Auxiliary measurement (for example, for sensor path auto-zero and/or sensor temperature) within the auxiliary measurement vector



Figure 23: SM+/AZ Configuration

For SM+/AZ configuration the measurement cycle and output update rate is shown in Figure 24 for an example of five enabled auxiliary measurement tasks. After finishing the SM+ main measurement task, firmware starts with data processing as described in section 5 and section 6. The resulting signal conditioning is written into the output registers.

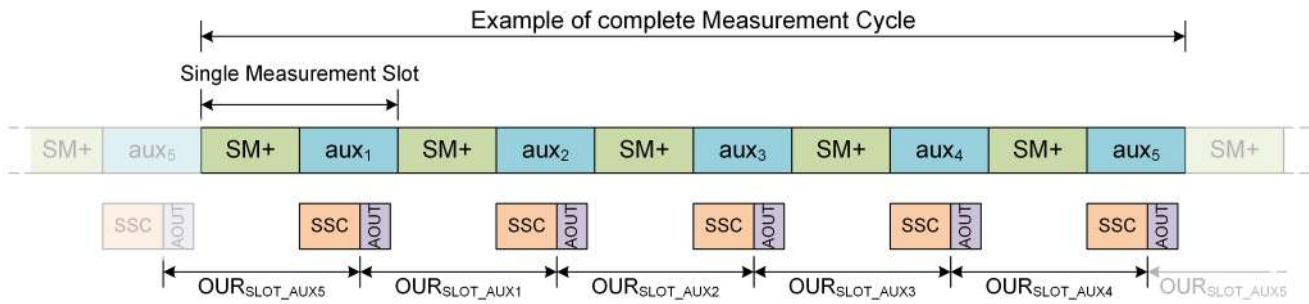


Figure 24: SM+/AZ Measurement Cycle and Output Update Rate



As shown in Figure 25, the worst-case latency consists of:

- 2 sensor AD-conversion times (duration depending on selected ADC resolution)
- 1 auxiliary conversion time (fixed duration, based on longest auxiliary conversion timing)
- 1 SSC calculation

Additionally there is a delay that depends on the selected interface:

- 1 settling time at AOUT for all analog output options
- 2 cycle times for IO-Link communication

Within the worst-case scenario it, consider that intermediate results can occur since input changes and data readout will be asynchron to the internal running measurement cycle.

Worst-case scenario for IO-Link communication depends on IO-Link master since it defines the cycle time. ZSSC3286 defines minimum cycle time of 600µs.

Assuming equal ADC resolution settings for the SM+/SM- configuration as described in subsection 4.6.3 and the SM+/AZ configuration described in this section, the worst case step response is shorter by two sensor AD-conversion times in case of the SM+/AZ setup. The auxiliary measurement duration in the SM+/AZ setup may become slightly longer than for the SM+/SM- configuration, since it is determined by the AZ measurement time if the selected resolution of the main bridge is larger than the resolutions of all other active auxiliary measurements. This is because the resolution of the AZ measurement is set by the resolution of the SM+ measurement and the longest measurement of the auxiliary measurement vector determines the duration of the aux<sub>i</sub> slot(s)

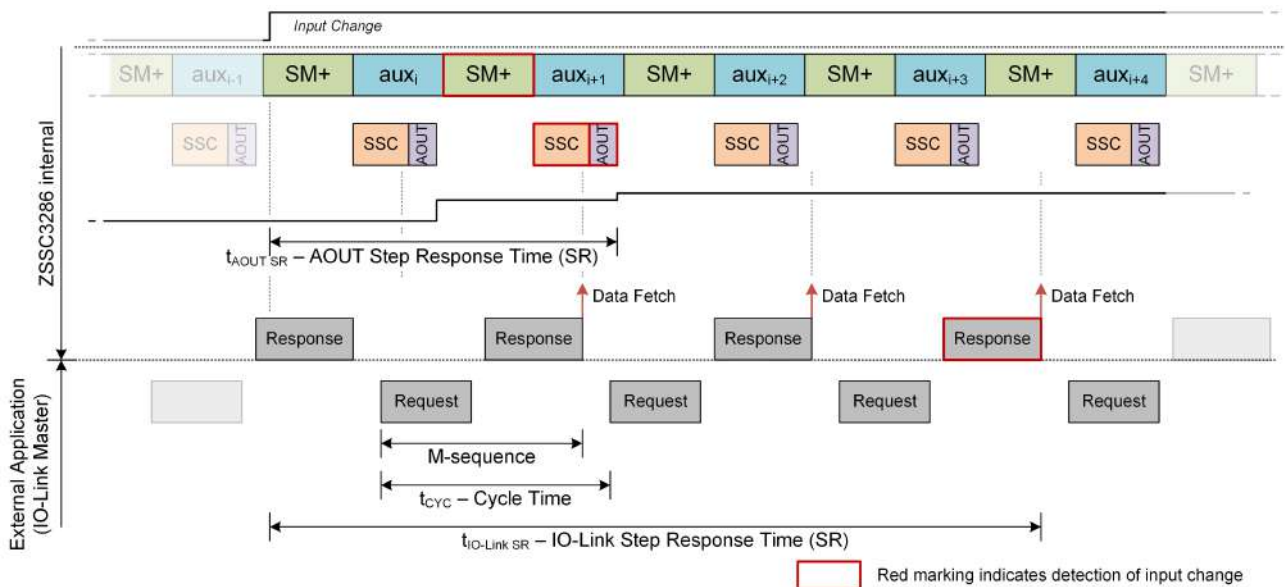


Figure 25: Measurement Flow and Latency for SM+/AZ Configuration

### 4.6.5 Accelerated Bridge Measurements with Sparsely Inserted Auxiliary Measurements

For applications which focus on highest conversion rates at the bridge sensor input but do not require a deterministic maximum input to output latency of the corrected sensor signal, auxiliary measurements can be sparsely inserted to occur only after a certain number of measurement sequences were executed by the AFE sequencer. This way, auxiliary measurements become executed even more seldom, giving the main sensor bridge measurements priority.

The AFE sequencer can be configured such that an  $aux_i$  measurement is only executed (inserted) after every  $P_x$  measurement sequence.  $P$  can be selected as 2, 4, or 8. Figure 26 shows an example of a measurement flow with  $P = 2$  while Figure 27 uses  $P = 8$  where  $aux_i$  measurements are executed after eighth measurement sequences.

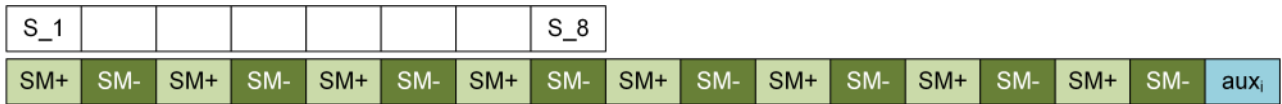


Figure 26: Auxiliary Measurement Executed after Every Second Measurement Cycle

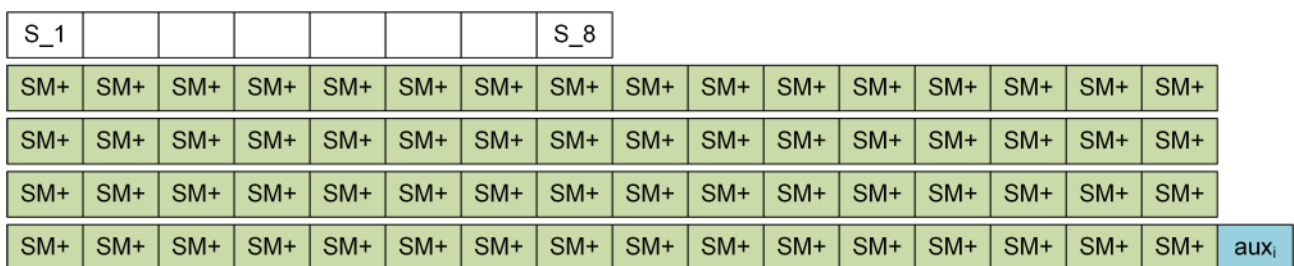


Figure 27: Sequencer Setup for Highest Update Rate on Bridge Sensor

For the use case of SM+/SM- measurement sequencer, the output update rate is shown in Figure 28. The complete measurement cycle is finished after finishing the last auxiliary measurement task. After finishing the SM+ main measurement task, firmware starts with data processing as described in section 5 and section 6. Since the auxiliary measurement tasks are inserted only after every 2nd, 4th, or 8th measurement sequence, the output update rate also varies in the same period. The same description is also valid if SM+/AZ only measurement sequencer is used.

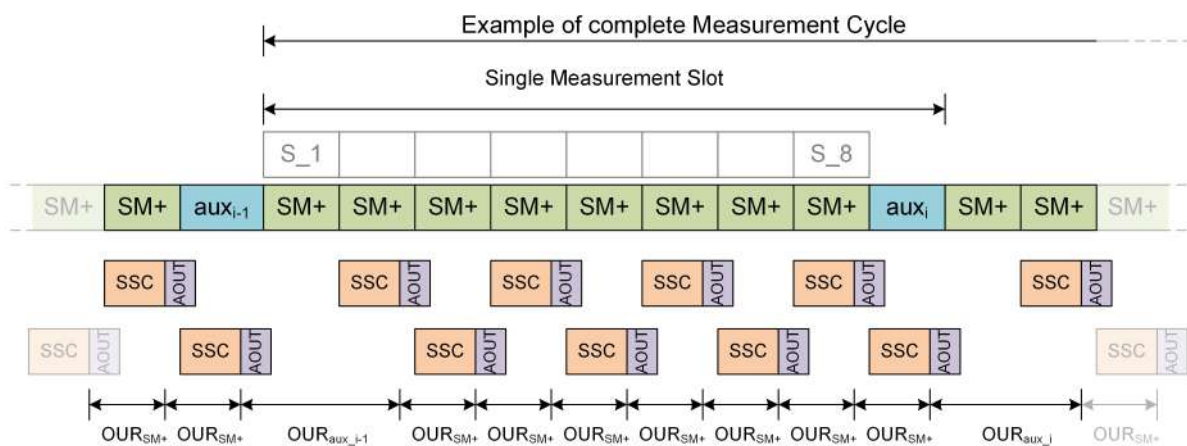


Figure 28: SM+ Accelerated Measurement Cycle and Output Update Rate

The worst case step response mainly depends on the selected AFE sequencer mode:

- SM+/SM- configuration: refer to Figure 22 and description for step response in subsection 4.6.3
- SM+/AZ configuration: refer to Figure 25 and description for step response in subsection 4.6.4

## 5 Sensor Signal Conditioning

### 5.1 Signal Conditioning Data Path

Figure 29 illustrates the sensor signal conditioning flow that is applied for AFE output data to compensate for offset, gain, non-linearity, and temperature effects and to calculate the conditioned data for further output processing. See subsection 5.2 to subsection 5.9 for more information on the basis mathematical subfunctions.

The signal path from conditioned data to individual output signals is described in section 6.

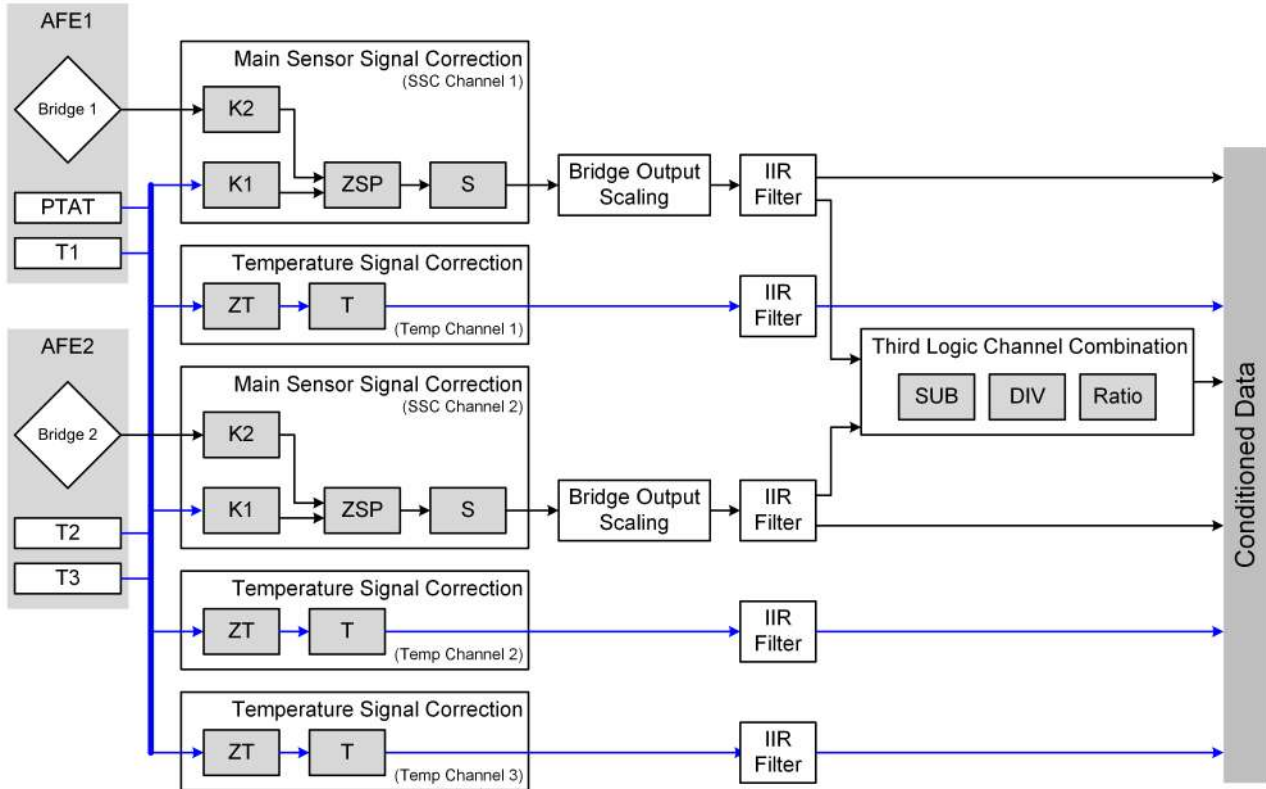


Figure 29: Sensor Signal Flow Chart from Input to Conditioned Data

### 5.2 Main Sensor Signal Correction

ZSSC3286 supports basic second-order compensation of sensor nonlinearities. The following basic SSC math options are available:

- Sensor signal correction
  - SOT Curve-0: Parabolic compensation curve
  - SOT Curve-1: S-shaped compensation curve
- Temperature signal correction

The parabolic compensation is recommended for most sensor types. The applied SSC math option can be selected in the GUI through the field Calibration\Curve.

The available SSC capabilities for SOT Curve-0 and SOT Curve-1 are described in Table 25, Table 26, and Table 27. The used equation terms are as follows:

|                                     |   |                                     |
|-------------------------------------|---|-------------------------------------|
| <i>S</i>                            | Corrected sensor reading output via I2C, OWI, or SPI  | Valid Input Range<br>0x0 to 0xFFFFF |
| <i>S_Raw</i>                        | Raw sensor reading from ADC (after AZ correction, depends on Afe1SmConfig)  | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>Gain_S</i>                       | Sensor gain term  | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>Offset_S</i>                     | Sensor offset term  | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>Tcg</i>                          | Temperature coefficient gain term   | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>Tco</i>                          | Temperature coefficient offset term   | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>T_Raw</i>                        | Raw temperature reading (after AZ correction)   | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>SOT_tcg</i>                      | Second-order term for Tcg non-linearity   | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>SOT_tco</i>                      | Second-order term for Tco non-linearity   | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>SOT_sens</i>                     | Second-order term for sensor non-linearity  | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>SENS_shift</i>                   | Post-calibration, post-assembly offset shift  | -(0x7FFFFFF) to 0x7FFFFFF           |
| ...                                 | Absolute value  |                                     |
| [...] <sup>ul</sup> / <sub>ll</sub> | Bound/saturation number range from ll to ul, overflow and/or underflow is reported as saturation in the Status Byte |                                     |

All raw data and compensation coefficients supplied to the formulas are required in 24-bit data format shown in Table 25 and Table 26.

**Table 25: Data Format of Raw ADC Readings**

| Bit Number         | 23              | 22              | 21              | 20              | ... | 2                | 1                | 0                |
|--------------------|-----------------|-----------------|-----------------|-----------------|-----|------------------|------------------|------------------|
| Meaning, Weighting | -2 <sup>0</sup> | 2 <sup>-1</sup> | 2 <sup>-2</sup> | 2 <sup>-3</sup> | ... | 2 <sup>-21</sup> | 2 <sup>-22</sup> | 2 <sup>-23</sup> |

**Table 26: Data Format of 24-bit SSC Coefficients**

| Bit Number         | 23                           | 22              | 21              | 20              | ... | 2                | 1                | 0                |
|--------------------|------------------------------|-----------------|-----------------|-----------------|-----|------------------|------------------|------------------|
| Meaning, Weighting | 0 = positive<br>1 = negative | 2 <sup>-1</sup> | 2 <sup>-2</sup> | 2 <sup>-3</sup> | ... | 2 <sup>-21</sup> | 2 <sup>-22</sup> | 2 <sup>-23</sup> |

The compensated result data is supplied in 24-bit data format as shown in Table 27.

**Table 27: Data Format of Corrected SSC Results (S and T)**

| Bit Number         | 23             | 22              | 21              | 20              | ... | 2                | 1                | 0                |
|--------------------|----------------|-----------------|-----------------|-----------------|-----|------------------|------------------|------------------|
| Meaning, Weighting | 2 <sup>0</sup> | 2 <sup>-1</sup> | 2 <sup>-2</sup> | 2 <sup>-3</sup> | ... | 2 <sup>-21</sup> | 2 <sup>-22</sup> | 2 <sup>-23</sup> |

### 5.3 Pre-calculation

Simplified:

$$K_1 = 2^{23} + \frac{T\_Raw}{2^{23}} \times \left( \frac{4 \times SOT\_tcg}{2^{23}} \times T\_Raw + 4 \times Tcg \right) \tag{1}$$

$$K_2 = 4 \times Offset\_S + S\_Raw + \frac{T\_Raw}{2^{23}} \times \left( \frac{4 \times SOT\_tco}{2^{23}} \times T\_Raw + 4 \times Tco \right) \tag{2}$$

Complete:

$$K_1 = \left[ 2^{23} + \left[ \frac{T\_Raw}{2^{23}} \times \left[ \left[ \frac{SOT\_tcg}{2^{21}} \times T\_Raw \right]_{-2^{25}}^{2^{25}-1} + 4 \times Tcg \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \tag{3}$$

$$K_2 = \left[ 4 \times Offset\_S + \left[ S\_Raw + \left[ \frac{T\_Raw}{2^{23}} \times \left[ \left[ \frac{SOT\_tco}{2^{21}} \times T\_Raw \right]_{-2^{25}}^{2^{25}-1} + 4 \times Tco \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \tag{4}$$

## 5.4 SOT Curve-0 (Parabolic Compensation)

Simplified:

$$Z_{SP} = \frac{4 \times Gain\_S}{2^{23}} \times \frac{K_1}{2^{23}} \times K_2 + 2^{23} \quad (5)$$

$$S = \frac{Z_{SP}}{2^{23}} \times \left( \frac{4 \times SOT\_sens}{2^{23}} \times Z_{SP} + 2^{23} \right) + SENS\_shift \quad (6)$$

**Note:**  $Z_{SP}$  and  $S$  are delimited to positive number range.

Complete:

$$Z_{SP} = \left[ \left[ \frac{Gain\_S}{2^{21}} \times \left[ \frac{K_1}{2^{23}} \times K_2 \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_0^{2^{25}-1} \quad (7)$$

$$S = \left[ \left[ \frac{Z_{SP}}{2^{23}} \times \left[ \left[ \frac{SOT\_sens}{2^{21}} \times Z_{SP} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + SENS\_shift \right]_0^{2^{24}-1} \quad (8)$$

## 5.5 SOT Curve-1 (S-shaped Compensation)

Simplified:

$$Z_{SS} = \frac{4 \times Gain\_S}{2^{23}} \times \frac{K_1}{2^{23}} \times K_2 \quad (9)$$

**Note:**  $K_1$  and  $K_2$  according to Equation 3 and Equation 4.

$$S = \frac{Z_{SS}}{2^{23}} \times \left( \frac{4 \times SOT\_sens}{2^{23}} \times |Z_{SS}| + 2^{23} \right) + 2^{23} + SENS\_shift \quad (10)$$

**Note:**  $S$  is delimited to positive number range.

Complete:

$$Z_{SS} = \left[ \frac{Gain\_S}{2^{21}} \times \left[ \frac{K_1}{2^{23}} \times K_2 \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \quad (11)$$

$$S = \left[ \left[ \left[ \frac{Z_{SS}}{2^{23}} \times \left[ \left[ \frac{SOT\_sens}{2^{21}} \times |Z_{SS}| \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} + SENS\_shift \right]_0^{2^{24}-1} \quad (12)$$

### 5.6 Temperature Signal Correction

Temperature is measured either internally by the ZSSC3286, through an additional external element, or by means of a combination of ZSSC3286 internal and external temperature sensing capabilities. Temperature correction contains both linear gain and offset terms as well as a second-order term to correct for any nonlinearities. For temperature, second-order compensation is always parabolic.

The correction equation terms are as follows:

|                 |   |                                     |
|-----------------|---|-------------------------------------|
| <i>T</i>        | Corrected temperature sensor reading output via digital interface | Valid Input Range<br>0x0 to 0xFFFFF |
| <i>T_Raw</i>    | Raw temperature reading after AZ correction                       | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>Gain_T</i>   | Gain coefficient for temperature                                  | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>Offset_T</i> | Offset coefficient for temperature                                | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>SOT_T</i>    | Second-order term for temperature source nonlinearity             | -(0x7FFFFFF) to 0x7FFFFFF           |
| <i>T_shift</i>  | Shift for post-calibration/post-assembly offset compensation      | -(0x7FFFFFF) to 0x7FFFFFF           |

The correction formula is best represented as a two-step process as follows:

Simplified:

$$Z_T = \frac{4 \times Gain\_T}{2^{23}} \times (T\_Raw + 4 \times Offset\_T) + 2^{23} \tag{13}$$

$$T = \frac{Z_T}{2^{23}} \times \left( \frac{4 \times SOT\_T}{2^{23}} \times Z_T + 2^{23} \right) \tag{14}$$

**Note:**  $Z_T$  and  $T$  are delimited to positive number range.

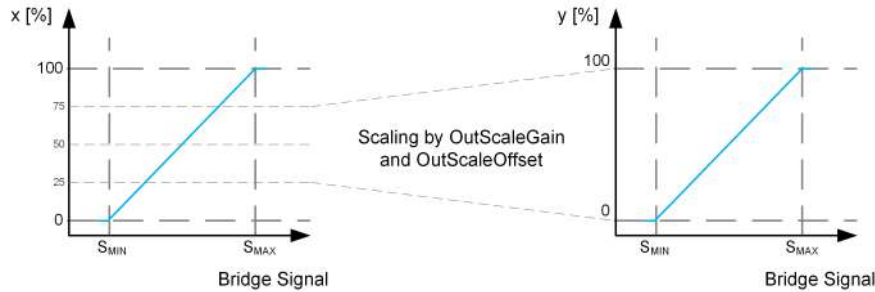
Complete:

$$Z_T = \left[ \left[ \frac{Gain\_T}{2^{21}} \times [T\_Raw + 4 \times Offset\_T]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_0^{2^{25}-1} \tag{15}$$

$$T = \left[ \left[ \frac{Z_T}{2^{23}} \times \left[ \left[ \frac{SOT\_T}{2^{21}} \times Z_T \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + T\_shift \right]_0^{2^{24}-1} \tag{16}$$

### 5.7 Bridge Output Scaling

ZSSC3286 offers a linear rescaling function to amplify or compress a partial region of the sensor input range to the desired signal output range. Figure 30 illustrates the rescaling on an example where the 25% to 75% calibrated signal input range is mapped to the output range of 0% to 100%. The feature is intended for customers who need to separate product derivatives after a common sensor calibration step.



**Figure 30: Example: Bridge Output Scaling Function for Scaling 25% - 75%, to final 0% - 100%**

The rescaling feature applies the following formula to the SSC conditioned outputs of the main bridge sensor:

$$y = \left[ \frac{8 \times OutScaleGain}{2^{23}} \times (x + 8 \times OutScaleOffset) \right]_{0}^{2^{24}-1} \tag{17}$$

The Coefficients *OutScaleGain* and *OutScaleOffset* are stored in the CCP (Configuration and Calibration Page) of ZSSC3286 in signed magnitude format. According to Table 28 *OutScaleGain* is limited to a maximum gain of 4 and the *OutScaleOffset* can vary from -1.5 to 0 related to the SSC result number range 0 to ~2.

**Table 28: Examples for Bridge Output Scaling**

| Input Relative – x [%] |       | OutScaleGain |                       | OutScaleOffset |                       | Output Relative – y [%] |     |
|------------------------|-------|--------------|-----------------------|----------------|-----------------------|-------------------------|-----|
|                        |       | real         | CCP Content (Decimal) | real           | CCP Content (Decimal) |                         |     |
| 0                      | 50.0  | 2.000        | 2097152               | 0.0            | 0                     | 0                       | 100 |
| 0                      | 33.3  | 3.003        | 3148876               | 0.0            | 0                     | 0                       | 100 |
| 0                      | 25.0  | 4.000        | 4194304               | 0.0            | 0                     | 0                       | 100 |
| 25                     | 50.0  | 4.000        | 4194304               | -0.5           | -524288               | 0                       | 100 |
| 25                     | 75.0  | 2.000        | 2097152               | -0.5           | -524288               | 0                       | 100 |
| 50                     | 100.0 | 2.000        | 2097152               | -1.0           | -1048576              | 0                       | 100 |
| 75                     | 100.0 | 4.000        | 4194304               | -1.5           | -1572864              | 0                       | 100 |

Table 29 lists the mapping of CCP register content to output scaling coefficients.

**Table 29: Data Format of Output Scaling Coefficients in CCP**

| Bit Number         | 23                           | 22             | 21             | 20             | 19              | ... | 1                | 0                |
|--------------------|------------------------------|----------------|----------------|----------------|-----------------|-----|------------------|------------------|
| Meaning, Weighting | 0 = positive<br>1 = negative | 2 <sup>2</sup> | 2 <sup>1</sup> | 2 <sup>0</sup> | 2 <sup>-1</sup> | ... | 2 <sup>-19</sup> | 2 <sup>-20</sup> |

The GUI supports the calculation of *OutScaleGain* and *OutScaleOffset* based on provided relative input and output range specifications (Can be configured on the GUI tab Configure\Output Scaling).

### 5.8 IIR Filter

The conditioned outputs of the two main sensor bridge channels CH1 and CH2 and the conditioned outputs of the temperature channels TCh1 to TCh3 can be low pass filtered for noise reduction. Each channel is equipped with an independent configurable IIR Filter. The mathematical filter description is as follows:

$$y_0 = x_0 \tag{18}$$

$$y_i = x_{i-1} + \frac{(x_i - y_{i-1}) \times Diff}{Avg} \tag{19}$$

where:

$$Diff = FiltDiff + 1 \tag{20}$$

$$Avg = 2^{FiltAvg} \tag{21}$$

*FiltDiff* and *FiltAvg* represent the filter coefficients which are stored as unsigned 3-bit values per filter channel in *IirFiltCoeffReg* inside the CCP of ZSSC3286. They are determined by the GUI (Configure\Filter) depending on the filter Tau selections made by the user. For a stable system, the  $Diff \leq Avg$  must be ensured.

The filter Tau can be calculated by:

$$\frac{Diff}{Avg} = \alpha \approx \frac{1}{\tau_{dig}} = \frac{\Delta T}{\tau_{ana}} \tag{22}$$

$$\tau_{dig} = -\frac{1}{\ln(1 - \alpha)} \tag{23}$$

$\tau_{dig}$  is given in number of digital samples.

### 5.9 Third Logic Channel Combination

The potentially pre-scaled and filtered two main sensor bridge channels Ch1 and Ch2 of ZSSC3286 can be mathematically combined to calculate the output of a third logic channel Ch3. Channel Ch3 is only available in the synchronized AFE mode which is enabled via the GUI menu Configure\AFE\Sequencer\AFE Selection and Configurability\selection: "AFE1+AFE2, config equally".

The calculation result on Ch3 is available through serial interface read out only. The digital output format is signed 32-bit (two's complement), see Table 30. Outputting the Ch3 result at AOUT is possible for subtraction and ratio only. Division is readable via digital interfaces only.

The Third Logic Channel (TLC) can be configured via the GUI menu Configure\TLC menu.

Following mathematical operations are available:

- Subtraction: (Ch1 – Ch2) or (Ch2 – Ch1)
- Division: (Ch1 / Ch2) or (Ch2 / Ch1)
- Ratio: If Ch1 == Ch2 then Ch3 = 1  
Else if Ch1 < Ch2 then Ch3 = Ch1 / Ch2  
Else Ch3 = 2 – (Ch2 / Ch1)

**Note:** Division calculation can lead to math saturation, which is not suppressed by firmware.

Calibration of the sensor channels Ch1 and Ch2 must still be done independently applying the single channel calibration routines.

**Table 30: Data Format of Logic Output Channel Ch3 at Serial Interface**

| Bit Number         | 31              | 30             | 29             | ... | 24             | 23             | 22              | 21              | ... | 2                | 1                | 0                |
|--------------------|-----------------|----------------|----------------|-----|----------------|----------------|-----------------|-----------------|-----|------------------|------------------|------------------|
| Meaning, Weighting | -2 <sup>8</sup> | 2 <sup>7</sup> | 2 <sup>6</sup> | ... | 2 <sup>1</sup> | 2 <sup>0</sup> | 2 <sup>-1</sup> | 2 <sup>-2</sup> | ... | 2 <sup>-21</sup> | 2 <sup>-22</sup> | 2 <sup>-23</sup> |



## 6 Post Processing Options for Conditioned Sensor Signals

### 6.1 Signal Post Processing Flow Chart

Figure 31 illustrates the signal flow from conditioned data to individual output signals. All basis mathematical sub-functions are described within the subsection 6.2, subsection 6.3 and subsection 6.4.

The signal path from AFE output data to conditioned data is described in subsection 5.2.

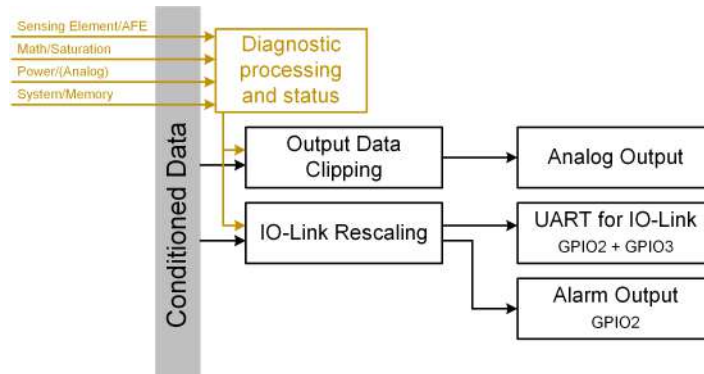


Figure 31: Sensor Signal Flow Chart from Input to Output

### 6.2 Output Data Clipping

The signaling of a diagnosis failure state can also be activated on the analog output AOUT via GUI tab Diagnostic\General. If the signalization of Diagnostic State at AOUT is enabled, discovered diagnostic failure states can be either mapped to the Upper or the Lower Diagnostic Range (UDR and LDR) of the output span (GUI tab Diagnostic\Sensor/AFE).

The boundaries of the upper and lower diagnostic ranges are configurable via the GUI tab Configure\Output Pre-process. They are typically set to 5% and 95% of the full scale output level but can be modified to the application needs.

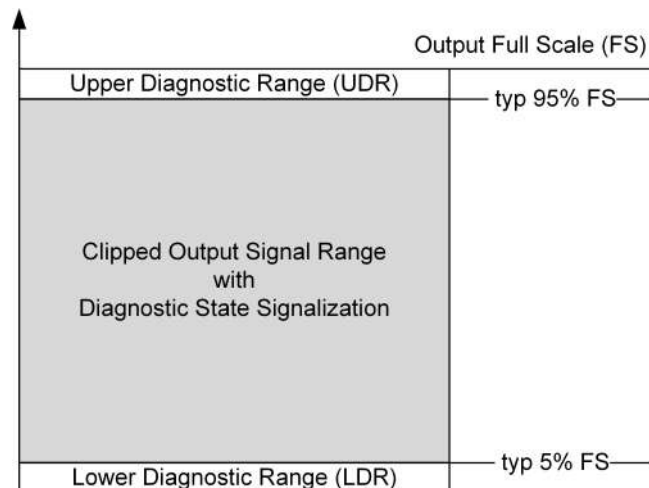


Figure 32: AOUT Output Ranges with Active Diagnostic State Signalization

To prevent false interpretation of very large or very low output signals (UDR and LDR ranges), the conditioned data is clipped to fit into the remaining output range between UDR and LDR before it is forwarded to the AOUT output.

**Note:** There is no rescaling of the conditioned data performed at this stage. If rescaling of the conditioned data to the clipped output signal range is required, use the Bridge Output Scaling feature (see subsection 5.7) or use different target values during the SSC calibration process.

### 6.3 IO-Link Rescaling

The purpose of rescaling is to implement a simple algorithm for scaling and offsetting the 24-bit SSC corrected data so that it can be provided in SI Units as the IO-Link Smart Sensor Profil (SSP) process data requests. As described in subsection 9.2 the ZSSC3286 features SSP 4.1.1.

Therefore all 24-bit SSC corrected data is shifted to 32-bit domain and then compensated by the following compensation mathematics and Equation 24:

|                    |  |  |
|--------------------|--|--|
| SSC                | Corrected 24-bit sensor signal selected for IO-Link Output | Valid Input Range<br>0x0 to 0xFFFFFFFF<br>-(0xFFFFFFFF) to 0xFFFFFFFF<br>-(0xFFFFFFFF) to 0xFFFFFFFF<br>-(0xFFFFFFFF) to 0xFFFFFFFF<br>0x0 to 0xFF |
| $SSC_{IO-Link}$    | Rescaled for IO-Link Output                                |  |
| $Gain_{Rescale}$   | Gain term for IO-Link rescaling                            |  |
| $Offset_{Rescale}$ | Offset term for IO-Link rescaling                          |  |
| $Offset\_Scalar$   | Offset shift for $Offset_{Rescale}$ parameter              |  |

The IO-Link rescaling is supported by the GUI within the tab IO-Link\SSP Scaling.

All data and compensation coefficients supplied to the formulas are required in the 32-bit data format described in Table 31, Table 32, Table 33, Table 34, and Equation 24.

**Table 31: Data Format of Corrected SSC Result**

| Bit Number         | 23    | 22       | 21       | 20       | ... | 2         | 1         | 0         |
|--------------------|-------|----------|----------|----------|-----|-----------|-----------|-----------|
| Meaning, Weighting | $2^0$ | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | ... | $2^{-21}$ | $2^{-22}$ | $2^{-23}$ |

**Table 32: Data Format of IO-Link rescaled Output for SSP 4.1.1**

| Bit Number         | 15       | 14       | 13       | 12       | ... | 2         | 1         | 0         |
|--------------------|----------|----------|----------|----------|-----|-----------|-----------|-----------|
| Meaning, Weighting | $-(2^0)$ | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | ... | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ |

**Table 33: Data Format of 32-bit  $Gain_{Rescale}$  and  $Offset_{Rescale}$  Coefficients**

| Bit Number         | 31                           | 30    | 29    | 28    | 27       | ... | 1         | 0         |
|--------------------|------------------------------|-------|-------|-------|----------|-----|-----------|-----------|
| Meaning, Weighting | 0 = positive<br>1 = negative | $2^2$ | $2^1$ | $2^0$ | $2^{-1}$ | ... | $2^{-27}$ | $2^{-28}$ |

**Table 34: Data Format of 8-bit  $Offset\_Scalar$  Coefficient**

| Bit Number         | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|--------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Meaning, Weighting | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |

$$SSC_{IO-Link} = (SSC \times 2^8 \times Gain_{Rescale}) + (Offset_{Rescale} \times Offset_{Scalar}) \tag{24}$$

### 6.4 Alarm Function

In SIO mode, the pin UART TxD (GPIO2) can be assigned a binary ALARM signal. this ALARM signal is output on C/Q line of IO-Link via the PHY as TxEN is always active in SIO mode.

Any Sensor Switching Channel from the IO-Link SSP can be mapped to the ALARM function. The ALARM switching behavior thus is completely dependent on IO-Link SSC configuration. The ALARM signal can be inverted before being output on pin UART TxD (GPIO2).

In Cyclic Mode, the ALARM signal will be constantly updated when new measurement results are available. In Command Mode, the last switching level is kept and output stays constantly. On Fallback from IO-Link COM Mode, the ALARM signal automatically will be output if the ALARM function is enabled in CCP. On WURQ, pin UART TxD automatically switches to IO-Link COM operation.

The activation and configuration of ALARM Function is done in CCP register 0x04 – IoMisc. For easy configuration, use the Renesas GUI in tab Configure\ALARM.

## 7 Sensor and System Diagnosis

The ZSSC3286 sensor and system diagnosis function can detect several false conditions on externally connected sensors and monitor long term gain and offset drifts of the analog front end. This makes ZSSC3286 well suited for sensing applications that require increased system reliability as well as for predictive maintenance supervision done by the host system.

### 7.1 Sensor and AFE Diagnostic Features

The supported sensor and AFE diagnostic features are summarized in Table 35.

**Table 35: Sensor and AFE Diagnosis Functions**

| Monitored Input or Component | Failure Category      | Failure Condition <sup>1</sup>  |
|------------------------------|-----------------------|---|
| Main sensor bridge 1         | INP or INN open       | INP to INN resistance >125kΩ  |
|                              | INP or INN shorted    | INP to INN resistance <170Ω   |
| Main sensor bridge 2         | INP or INN open       | INP to INN resistance >125kΩ  |
|                              | INP or INN shorted    | INP to INN resistance <170Ω   |
| Temperature sensor T1        | Short to Top (TOP)    | T1 to TOP resistance <500Ω  |
|                              | Short to Bottom (BOT) | T1 to BOT resistance <500Ω  |
|                              | Open                  | T1 resistance >2MΩ, 500kΩ, 100kΩ  |
| Temperature sensor T2        | Short to Top (TOP)    | T2 to TOP resistance <500Ω  |
|                              | Short to Bottom (BOT) | T2 to BOT resistance <500Ω  |
|                              | Open                  | T2 resistance >2MΩ, 500kΩ, 100kΩ  |
| Temperature sensor T3        | Short to Top (TOP)    | T3 to TOP resistance <500Ω  |
|                              | Short to Bottom (BOT) | T3 to BOT resistance <500Ω  |
|                              | Open                  | T3 resistance >2MΩ, 500kΩ, 100kΩ  |
| AFE1                         | Gain Drift            | Gain check deviates by provided percentage from previously stored reference value   |
|                              | Offset Drift          | Offset check deviates by provided permillage from previously stored reference value |
| AFE2                         | Gain Drift            | Gain check deviates by provided percentage from previously stored reference value   |
|                              | Offset Drift          | Offset check deviates by provided permillage from previously stored reference value |

<sup>1</sup> Typical values. Further specifications are provided in Table 8.

For all active sensor inputs and AFEs, the checks can be enabled selectively on the GUI tab Diagnostic\Sensor/AFE. The AFE gain drift check employs an internally connected resistive DAC to create itself a defined input signal. The internal DAC can generate four different input voltages: 2mV, 10mV, 100mV, 200mV. The GUI proposes the most suitable setting based on other configurations made for the AFE. The selected voltage level is stored in the CCP.

In order to make proper use of the long-term AFE gain and offset drift checks, a device dependent reference value must be acquired and stored during the sensor calibration process. The GUI supports this via the 'Get' button which is located in front of the GainRef and OffsetRef fields.

To run single tests for sensor and AFE diagnosis features, 0xB4 command can be used which triggers a single measurement returning a pass or fail criteria as shown in Table 36

Table 36: Self Diagnostic Measurement Command

| Command Code            | Description   | Return                |
|-------------------------|---|-----------------------|
| 0xB4 followed by 0x0XYY | <b>Self-Diagnostic Measure</b> for AFE1 and AFE2 <ul style="list-style-type: none"> <li>• 0x0X <ul style="list-style-type: none"> <li>◦ AFE1: 0x00</li> <li>◦ AFE2: 0x01</li> </ul> </li> <li>• 0xYY - see below</li> </ul> | 2 Bytes               |
| 0xYY                    | Measurement   | Return                |
| 0x05                    | External temperature sensor, T1, check short to top   | 0b0000_0000_0000_000X |
| 0x06                    | External temperature sensor, T1, check short to bottom  | 0b0000_0000_0000_000X |
| 0x07                    | External temperature sensor, T1, check open   | 0b0000_0000_0000_000X |
| 0x0A                    | External temperature sensor, T2, check short to top   | 0b0000_0000_0000_000X |
| 0x0B                    | External temperature sensor, T2, check short to bottom  | 0b0000_0000_0000_000X |
| 0x0C                    | External temperature sensor, T2, check open   | 0b0000_0000_0000_000X |
| 0x0F                    | External temperature sensor, T3 (pin GUARD), check short to top   | 0b0000_0000_0000_000X |
| 0x10                    | External temperature sensor, T3 (pin GUARD), check short to bottom  | 0b0000_0000_0000_000X |
| 0x11                    | External temperature sensor, T3 (pin GUARD), check open   | 0b0000_0000_0000_000X |
| 0x1B                    | Main bridge sensor connection check open  | 0b0000_0000_0000_000X |
| 0x1C                    | Main bridge sensor connection check short   | 0b0000_0000_0000_000X |
| 0x27                    | Offset drift (calculated diagnosis result)  | 0b0000_0000_0000_000X |
| 0x28                    | Gain drift (calculated diagnosis result)  | 0b0000_0000_0000_000X |

## 7.2 Sensor and System Diagnosis Status

All individual sensor and AFE diagnosis features are able to set an individual bit inside a Fault Memory.

Fault Memory is a nonvolatile memory that tracks all diagnosis bits until they are actively cleared. Clearing is possible only via ClearFaultMem (0xB9) command or a system reset. Thus before checking system diagnosis it is recommend to clear the fault memory. The fault memory can be read via RdFaultMem (0xB8) command. Reading the Fault Memory returns three words as shown in Table 37 to Table 39

Updating the Fault Memory is possible via command 0xB2.

Table 37: Fault Memory - Word 0 - Bits 31:0

| Bits    | Description  | Bits | Description  |
|---------|--|------|--|
| 31 : 25 | Reserved   | 11   | AFE2 sensor signal range check: INP2   |
| 24      | AFE2 temperature sensor shorted connection check<br>→ T3 – BOT shorted: $R < R_{T\_SHORT}$ | 10   | AFE2 sensor leakage check: INN2 to VSS   |
| 23      | AFE2 temperature sensor shorted connection check<br>→ T3 – TOP shorted: $R < R_{T\_SHORT}$ | 9    | AFE2 sensor leakage check: INP2 to VSS   |
| 22      | AFE2 temperature sensor broken connection check<br>→ T3 open: $R > R_{T\_OPEN}$            | 8    | AFE2 sensor shorted connection check<br>→ INP2 – INN2 shorted: $R < R_{short}$ |
| 21      | AFE2 temperature sensor shorted connection check<br>→ T2 – BOT shorted: $R < R_{T\_SHORT}$ | 7    | AFE2 sensor broken connection check<br>→ INP2 or INN2 open: $R > R_{broken}$   |
| 20      | AFE2 temperature sensor shorted connection check<br>→ T2 – TOP shorted: $R < R_{T\_SHORT}$ | 6    | AFE1 sensor signal range check: INN1   |
| 19      | AFE2 temperature sensor broken connection check<br>→ T2 open: $R > R_{T\_OPEN}$            | 5    | AFE1 sensor signal range check: INP1   |
| 18      | AFE1 temperature sensor shorted connection check<br>→ T1 – BOT shorted: $R < R_{T\_SHORT}$ | 4    | AFE1 sensor leakage check: INN1 to VSS   |
| 17      | AFE1 temperature sensor shorted connection check<br>→ T1 – TOP shorted: $R < R_{T\_SHORT}$ | 3    | AFE1 sensor leakage check: INP1 to VSS   |
| 16      | AFE1 temperature sensor broken connection check<br>→ T1 open: $R > R_{T\_OPEN}$            | 2    | AFE1 sensor shorted connection check<br>→ INP1 – INN1 shorted: $R < R_{short}$ |
| 15 : 13 | Reserved   | 1    | AFE1 sensor broken connection check<br>→ INP1 or INN1 open: $R > R_{open}$     |
| 12      | AFE2 sensor signal range check: INN2   | 0    | Reserved   |

Table 38: Fault Memory - Word 1 - Bits 31:0

| Bits   | Description       |
|--------|-------------------|
| 31 : 4 | Reserved          |
| 3      | AFE2 Offset Drift |
| 2      | AFE2 Gain Drift   |
| 1      | AFE1 Offset Drift |
| 0      | AFE1 Gain Drift   |

Table 39: Fault Memory - Word 2 - Bits 31:0

| Bits   | Description   |
|--------|---|
| 31 : 6 | Reserved  |
| 5      | SSC calculation unit OR raw output data saturation channel 1, bridge sensor data      |
| 4      | SSC calculation unit OR raw output data saturation channel 1, temperature sensor data |
| 3      | SSC calculation unit OR raw output data saturation channel 2, bridge sensor data      |
| 2      | SSC calculation unit OR raw output data saturation channel 2, temperature sensor data |
| 1      | SSC calculation unit channel 3, bridge sensor data                                    |
| 0      | SSC calculation unit OR raw output data saturation channel 3, temperature sensor data |

## 8 Analog Output

The conditioned and post processed output data of one of the following channels can be made available as analog output signal at the Analog Output AOUT

- Bridge Sensor Channel 1
- Bridge Sensor Channel 2
- Third Logic Channel
- Temperature Channel 1
- Temperature Channel 2
- Temperature Channel 3

Depending on the configuration of the Analog Output Driver, two different output modes, (absolute voltage output and current mode output) are supported.

### 8.1 Analog Output Driver

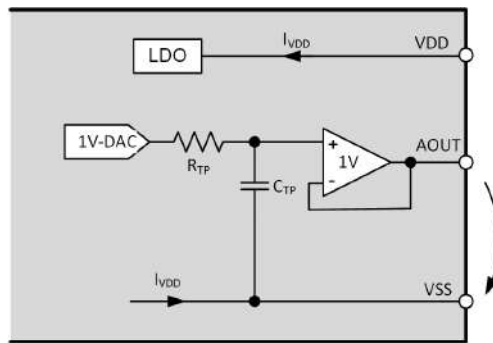


Figure 33: Block Schematic AOUT Driver

The Analog Output Driver is a buffer for a full scale voltage of 1V. The following functional assignments apply:

- 1V absolute Voltage Mode
- 3-wire Current Loop Mode
- 5V absolute Voltage Mode (with external amplifier)
- 10V absolute Voltage Mode (with external amplifier)

Depending on the functional assignment and on the System Mode, the Analog Output Driver is set to the states shown in Table 40.

Table 40: Analog Output Driver States

| System Mode              | SIO Mode                                | IO-Link COM Mode                       |
|--------------------------|---|--|
| Disabled Mode            | floating                                | floating                               |
| Absolute Voltage Mode    | voltage following SSC value             | 0V                                     |
| 3-Wire Current Loop Mode | voltage for current following SSC value | voltage for minimum current (typ. 4mA) |

### 8.2 Negative Voltage Generation for AOUT

To support True-0V signals on the Analog Output (AOUT), ZSSC3286 provides an option to externally supply a negative voltage rail for the AOUT buffer at VDDN. VDDN supply specifications are shown in Table 41. The external circuitry must ensure to not generate a VDDN voltage of less than -0.5V to prevent latchup conditions for the internal circuitry.

The negative VDDN voltage can also be generated by an internal charge pump circuit. Its maximum current can be adjusted.

The activation of the internal charge pump at VDDN considerably increases the power consumption of ZSSC3286 and needs to be carefully considered in applications where current consumption of the sensor device (sensing element + ZSSC3286) is a critical parameter. The VDDN charge pump can only be used for  $VDD \geq 2.7V$ .

If no True-0V signals are required at AOUT, the user must disable the VDDN charge pump in the GUI and directly connect VDDN with VSS on PCB level.

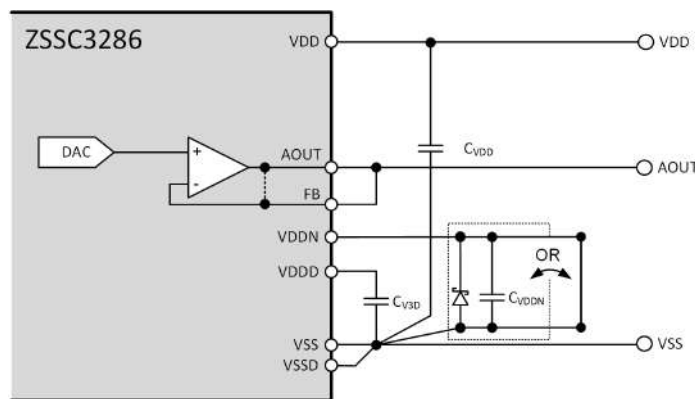
The charge pump function is only available for Voltage Output mode. The charge pump circuit requires an external buffer capacitor  $C_{VDDN}$  and a Schottky Diode to work properly.

**Table 41: Parameter Negative Voltage for AOUT**

| Symbol            | Parameter   | Conditions  | Minimum | Typical           | Maximum | Units   |
|-------------------|---|---|---------|-------------------|---------|---------|
| $VDD_{CP}$        | VDD operating range of internal charge pump       |   | 2.7     |                   | 5.5     | V       |
| VDDN              | Negative voltage supply for analog output (AOUT)  | Internally generated, requires activation of VDDN charge pump |         | $V_{ExtSchottky}$ |         | V       |
|                   |   | Externally supplied   | 0       | -0.3V             | -0.5V   | V       |
| $I_{VDDN}$        | Available charge pump load current                | Programmable in 4 steps.                                      |         |                   | 0.5     | mA      |
|                   |   |   |         |                   | 1       |         |
|                   |   |   |         |                   | 3       |         |
|                   |   |   |         |                   | 5       |         |
| $I_{VDD}$         | Additional charge pump current consumption at VDD | 0.5mA load current  | 0.5     | 4.5               | 5       | mA      |
|                   |   | 1.0mA load current  | 1       | 9                 | 10      |         |
|                   |   | 3.0mA load current  | 3       | 15.5              | 17      |         |
|                   |   | 5.0mA load current  | 5       | 25                | 30      |         |
| $C_{VDDN}$        | Buffer capacitance at pin VDDN                    |   |         | 1                 |         | $\mu F$ |
| $V_{FW-Schottky}$ | Forward voltage of external Schottky diode        |   |         | 0.3               | 0.5     | V       |

### 8.3 Analog Output Configuration

#### 8.3.1 1V Absolute Output Voltage Mode



**Figure 34: 1V Absolute Output Voltage Configuration at AOUT**

The SSC output can be mapped to 0V to 1V voltage range with the application circuit shown in Figure 34 and activation of the 1V absolute Voltage Mode.

The applied reference voltage for the AOUT DAC is generated from an internal factory calibrated bandgap source.

8.3.2 Absolute Voltage Mode – External Amplification

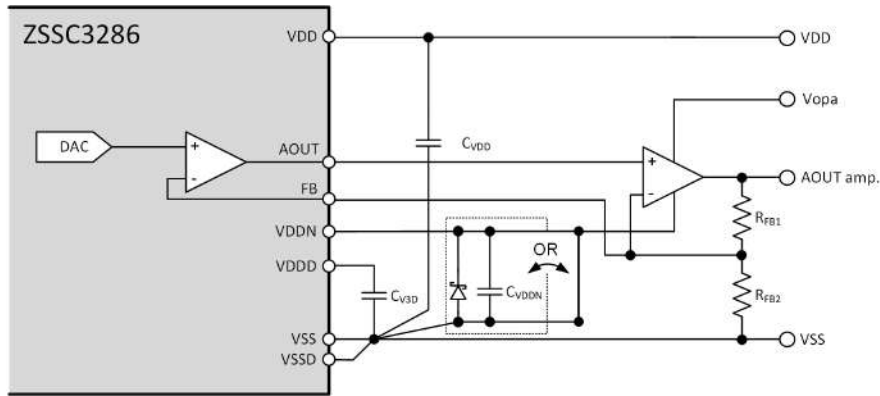


Figure 35: 5V Absolute Output Voltage Configuration at AOUT

Using an external operational amplifier, the 1V absolute voltage output can be scaled to higher voltages, for example 5V or 10V output. The application circuit is shown in Figure 35. The Feedback Pin FB should be connected to the inverting input of the external operational amplifier for better voltage accuracy. The external operational amplifier should be offset compensated. The external voltage amplification factor calculates as follows:

$$A = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \tag{25}$$

8.3.3 3-Wire Current Loop Mode

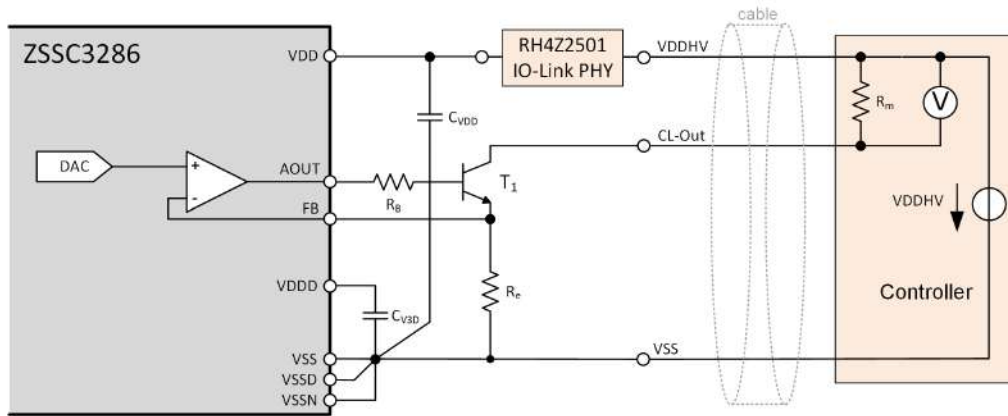


Figure 36: 3-wire NPN Current Loop Configuration at AOUT

Table 42: External Components in 3-Wire Current Loop Mode

| Symbol | Parameter          | Minimum              | Typical | Maximum | Units    |
|--------|--------------------|----------------------|---------|---------|----------|
| $R_e$  | Emitter resistor   |                      | 43      |         | $\Omega$ |
| $R_b$  | Base resistor      |                      | 4700    |         | $\Omega$ |
| $T_1$  | Bipolar Transistor | for example BCX56-16 |         |         | n.a.     |

The SSC output can be mapped to an input current at CL-Out in the application circuit shown in Figure 36 and by activation of the 3-Wire Current Loop Mode.

The signal current at CL-Out is typically required to range from 4mA to 20mA. The available min/max signal current range at CL-Out depends on the actual value of the external emitter resistor  $R_e$ .

To compensate for tolerances of  $R_e$ , the GUI offers a post calibration option to calibrate the current loop current to the required absolute accuracy (currently only available via I2C).



## 9 Digital Interfaces

### 9.1 Serial Interfaces

The ZSSC3286 features three digital interface protocols, shown in Table 43.

**Table 43: Digital Interface Protocols**

| Protocol           | Mode   | Function   |
|--------------------|--------|--|
| IO-Link (via UART) | Device | Sensor data read out, SSC configuration and calibration, FW Update |
| I2C                | Slave  | Sensor data read out, SSC configuration and calibration, FW Update |
| OWI                | Master | Only for configuring the RH4Z2501 IO-Link PHY                      |

Digital slave / device interfaces do not initiate data communication with the master system themselves but react on arbitrary received read/write requests from the master. I2C and IO-Link (COM mode) cannot be active at the same time.

After power up, the ZSSC3286 starts in SIO mode. In SIO mode, I2C communication is available. When a WURQ is received, the ZSSC3286 switches to IO-Link COM mode (refer to Figure 5).

### 9.2 UART (IO-Link)

The ZSSC3286 implements a UART interface for realization of IO-Link (SDCI) communication when connected to an IO-Link PHY (for example RH4Z2501, Reference 3, complying to the following standards:

- UART Rx/D
- UART Tx/D
- WU PHY
- TxEN PHY
- OWI /SS PHY

For connection to the PHY, the following pins are used:

- IO-Link Interface and System Specification V1.1.3 (Reference 1)
- IO-Link Common Profile Specification V1.1 (Reference 2)
- IO-Link Profile Smart Sensors 2nd Edition Specification V1.1
- IO-Link Profile BLOB Transfer & Firmware Update Specification V1.1
- IODD IO Device Description Specification V1.1.3

The ZSSC3286 only supports COM3 SDCI communication mode with transmission rate of 230.4kbit/s at a cycle time of 600µs. It features the Smart Sensor Profile (SSP) 4.1.1 (Profile-ID 0x0010, Process Data Structure PDI32.MSDC32\_1). The ZSSC3286 supports the ISDUs listed in Table 44 to Table 65.

## 9.2.1 Direct Parameter Page 1

Table 44: Communication Control

| ISDU Index | ISDU Sub-Index | Name                 | Access | Datatype / (Default Value) | Further Info   | IO-Link Operation Mode |                            |
|------------|----------------|----------------------|--------|----------------------------|--|------------------------|----------------------------|
|            |                |                      |        |                            |  | Bootloader             | COM Mode (Active Firmware) |
| 0x0        | 0x1            | MasterCommand        | W      | UIntegerT8 / (n.a.)        |  | x                      | x                          |
|            | 0x2            | MasterCycleTime      | RW     | UIntegerT8 / (0x0)         | Defined by IO-Link master  | x                      | x                          |
|            | 0x3            | MinCycleTime         | R      | UIntegerT8 / (0x6)         | 600µs minimum cycle time for SSP 4.1.1   |                        | x                          |
|            | 0x3            | MinCycleTime         | R      | UIntegerT8 / (0x16)        | 2200µs minimum cycle time  | x                      |                            |
|            | 0x4            | M-sequenceCapability | R      | UIntegerT8 / (0x2B)        | <ul style="list-style-type: none"> <li>ISDU support bit set</li> <li>OPERATE with 2 bytes of on-request data</li> <li>PRE-OPERATE with 8 bytes of on-request data</li> </ul> |                        | x                          |
|            | 0x4            | M-sequenceCapability | R      | UIntegerT8 / (0x2D)        | <ul style="list-style-type: none"> <li>ISDU support bit set</li> <li>OPERATE with 8 bytes of on-request data</li> <li>PRE-OPERATE with 8 bytes of on-request data</li> </ul> | x                      |                            |
|            | 0x5            | RevisionID           | RW     | UIntegerT8 / (0x11)        | IO-Link protocol V1.1  | x                      | x                          |
|            | 0x6            | ProcessDataIn        | R      | UIntegerT8 / (0x83)        | SSP 4.1.1: <ul style="list-style-type: none"> <li>SIO-bit not set (0)</li> <li>4 bytes of Process Data</li> </ul> SIO-bit depends on ALARM feature setting.                  |                        | x                          |
|            | 0x6            | ProcessDataIn        | R      | UIntegerT8 / (0x0)         | No Process Data in bootloader.   | x                      |                            |
|            | 0x7            | ProcessDataOut       | R      | UIntegerT8 / (0x0)         | n.a. for sensors, only for actuators   | x                      | x                          |

Table 45: Identification

| ISDU Index | ISDU Sub-Index | Name                      | Access | Datatype / (Default Value) | Further Info   | IO-Link Operation Mode |                            |
|------------|----------------|---------------------------|--------|----------------------------|--|------------------------|----------------------------|
|            |                |                           |        |                            |  | Bootloader             | COM Mode (Active Firmware) |
| 0x0        | 0x8            | VendorID 1 (Octet 1, MSB) | R      | UIntegerT8 / (0x1)         | Renesas vendor ID: 396<br><b>Note:</b> Modifiable via CCP  | x                      | x                          |
|            | 0x9            | VendorID 2 (Octet 0, LSB) |        | UIntegerT8 / (0x8C)        |  |                        |                            |
|            | 0xA            | DeviceID 1 (Octet 2, MSB) | RW     | UIntegerT8 / (0x0)         | Value 0x0 is not permitted. Values for Active Firmware and Bootloader shall be different. Write attempt to this parameter has no effect (compatibility mode not supported).<br><b>Note:</b> Modifiable via CCP |                        | x                          |
|            | 0xB            | DeviceID 2 (Octet 1)      |        | UIntegerT8 / (0x0)         |  |                        |                            |
|            | 0xC            | DeviceID 3 (Octet 0, LSB) |        | UIntegerT8 / (0x1)         |  |                        |                            |
|            | 0xA            | DeviceID 1 (Octet 2, MSB) | RW     | UIntegerT8 / (0x0)         | Value 0x0 is not permitted. Values for Active Firmware and Bootloader shall be different. Write attempt to this parameter has no effect (compatibility mode not supported).<br><b>Note:</b> Modifiable via CCP | x                      |                            |
|            | 0xB            | DeviceID 2 (Octet 1)      |        | UIntegerT8 / (0x0)         |  |                        |                            |
|            | 0xC            | DeviceID 3 (Octet 0, LSB) |        | UIntegerT8 / (0x2)         |  |                        |                            |
|            | 0xD            | FunctionID 1 (MSB)        | R      | UIntegerT8 / (0x0)         | value 0x0 by specification   | x                      | x                          |
|            | 0xE            | FunctionID 2 (LSB)        |        |                            |  |                        |                            |

## 9.2.2 System

Table 46: System

| ISDU Index | ISDU Sub-Index | Name          | Access | Datatype / (Default Value) | Further Info  | IO-Link Operation Mode |                            |
|------------|----------------|---------------|--------|----------------------------|---|------------------------|----------------------------|
|            |                |               |        |                            |   | Bootloader             | COM Mode (Active Firmware) |
| 0x2        | 0x0            | SystemCommand | W      | UIntegerT8 / (n.a)         | See supported commands in Table 47, Table 48, Table 49, Table 50 and Table 51 | x                      | x                          |

The following SystemCommands listed in Table 47, Table 48, Table 49, Table 50, and Table 51 are supported:

Table 47: System Commands - Block Parametrization

| System Command | Name               | Further info  | IO-Link Operation Mode |          |
|----------------|--------------------|---|------------------------|----------|
|                |                    |   | Bootloader             | COM Mode |
| 0x1            | ParamUploadStart   |   |                        | x        |
| 0x2            | ParamUploadEnd     |   |                        | x        |
| 0x3            | ParamDownloadStart |   |                        | x        |
| 0x4            | ParamDownloadEnd   |   |                        | x        |
| 0x5            | ParamDownloadStore | Command used to finalize parametrization or to start Data Storage |                        | x        |
| 0x6            | ParamBreak         |   |                        | x        |

Table 48: System Commands - Device Reset

| System Command | Name             | Further info   | IO-Link Operation Mode |          |
|----------------|------------------|--|------------------------|----------|
|                |                  |  | Bootloader             | COM Mode |
| 0x80           | DeviceReset      |  | x                      | x        |
| 0x81           | ApplicationReset | <ul style="list-style-type: none"> <li>• reset of application-specific parameters</li> <li>• identification parameters stay unchanged</li> <li>• uninterrupted communication with Master</li> </ul>        |                        | x        |
| 0x83           | BackToBox        | <ul style="list-style-type: none"> <li>• reset of application-specific parameters and identification parameters</li> <li>• Device must be power cycled to reestablish communication with Master</li> </ul> |                        | x        |

**Note:** Commands in Table 49 are only available if Locator function is enabled in CCP.

Table 49: System Commands - Locator

| System Command | Name         | Further info   | IO-Link Operation Mode |          |
|----------------|--------------|--|------------------------|----------|
|                |              |  | Bootloader             | COM Mode |
| 0x7E           | LocatorStart | Locator sequence restarts in case this command is issued before completion of the previous locator sequence. |                        | x        |
| 0x7F           | LocatorStop  | no effect if locator sequence is not in progress   |                        | x        |

Table 50: System Commands - Firmware Update

| System Command | Name        | Further info             | IO-Link Operation Mode |          |
|----------------|-------------|--------------------------|------------------------|----------|
|                |             |                          | Bootloader             | COM Mode |
| 0x50           | BM_UNLOCK_S | Start unlocking sequence |                        | x        |
| 0x51           | BM_UNLOCK_F | Unlocking command 1      |                        | x        |
| 0x52           | BM_UNLOCK_T | Unlocking command 2      |                        | x        |
| 0x53           | BM_ACTIVATE | Activates new firmware   | x                      |          |

Table 51: System Commands - Teach

| System Command | Name          | Further info | IO-Link Operation Mode |          |
|----------------|---------------|--------------|------------------------|----------|
|                |               |              | Bootloader             | COM Mode |
| 0x40           | TeachApply    |              |                        | x        |
| 0x41           | TeachSP1      |              |                        | x        |
| 0x42           | TeachSP2      |              |                        | x        |
| 0x43           | TeachSP1TP1   |              |                        | x        |
| 0x44           | TeachSP1TP2   |              |                        | x        |
| 0x45           | TeachSP2TP1   |              |                        | x        |
| 0x46           | TeachSP12TP2  |              |                        | x        |
| 0x47           | TeachSP1Start |              |                        | x        |
| 0x48           | TeachSP1Stop  |              |                        | x        |
| 0x49           | TeachSP2Start |              |                        | x        |
| 0x4A           | TeachSP2Stop  |              |                        | x        |
| 0x4F           | TeachCancel   |              |                        | x        |

Table 52: DataStorageIndex

| ISDU Index | ISDU Sub-Index | Name               | Access | Datatype / (Default Value) | Further Info   | IO-Link Operation Mode |                            |
|------------|----------------|--------------------|--------|----------------------------|--|------------------------|----------------------------|
|            |                |                    |        |                            |  | Bootloader             | COM Mode (Active Firmware) |
| 0x3        | 0x1            | DS_Command         | RW     | UIntegerT8 / (n.a.)        |  |                        | x                          |
|            | 0x2            | State_Property     | R      | UIntegerT32 / (n.a.)       |  |                        | x                          |
|            | 0x3            | Data_Storage_Size  | R      | UIntegerT32 / (n.a.)       | sum of the size of all parameters plus 4 bytes per parameter   |                        | x                          |
|            | 0x4            | Parameter_Checksum | R      | UIntegerT32 / (n.a.)       |  |                        | x                          |
|            | 0x5            | Index_List         | R      | UIntegerT8[N] / (n.a.)     | <p><math>N = (\text{parameter count} \times 3) + 2</math></p> <p>index list contains three bytes for each ISDU parameter that is handled by the data storage mechanism:</p> <ul style="list-style-type: none"> <li>• upper 8bit of ISDU index</li> <li>• lower 8bit of ISDU index</li> <li>• subindex (usually 0x0)</li> </ul> <p>The index list ends with a termination marker of two zero bytes.</p> <p>It does not cover all parameters that are part of the parameter flash structure.</p> <p>The index list is fixed for any specific DeviceID.</p> |                        | x                          |

**Note:** Table 53 column “ISDU Sub-Index” commands are not directly accessible. All parameter values within the ISDU Index are returned when sending command containing the ISDU Index with Sub-Index 0x0.

**Table 53: ProfileCharacteristic**

| ISDU Index | ISDU Sub-Index | Name   | Access | Datatype / (Default Value)                       | Further Info   | IO-Link Operation Mode |                            |
|------------|----------------|--|--------|--|--|------------------------|----------------------------|
|            |                |  |        |  |  | Bootloader             | COM Mode (Active Firmware) |
| 0xD        | 0x1            | SSP: Measuring and Switching Sensor, 1 channel                       | R      | UIntegerT16 / (0x10)                             | SSP 4.1.1  |                        | x                          |
|            | 0x1            | BLOB transfer  | R      | UIntegerT16 / (0x30)                             | BLOB transfer is used for CCP update.  | x                      |                            |
|            | 0x2            | Firmware Update Profile  | R      | UIntegerT16 / (0x31)                             |  | x                      | x                          |
|            | 0x3            | Identification and Diagnosis Profile                                 | R      | UIntegerT16 / (0x4000)                           |  |                        | x                          |
|            | 0x4            | Two Value Teach Function Class                                       | R      | UIntegerT16 / (0x8011)                           |  |                        | x                          |
|            | 0x5            | Dynamic Teach Function Class   | R      | UIntegerT16 / (0x8012)                           |  |                        | x                          |
|            | 0x6            | Object Detection Function Class or Quantity Detection Function Class | R      | UIntegerT16 / (0x8013) or UIntegerT16 / (0x8014) | Switching Scheme configured via CCP<br><b>Note:</b> Modifiable via CCP (default: quantity detection)                     |                        | x                          |
|            | 0x7            | Locator Function Class   | R      | UIntegerT16 / (0x8101)                           | Provides visual recognition of the Device<br><b>Note:</b> Subindex available only if Locator Function is enabled in CCP. |                        | x                          |

**Table 54: PDInputDescriptor**

| ISDU Index | ISDU Sub-Index | Name          | Access | Datatype / (Default Value) | Further Info   | IO-Link Operation Mode |                            |
|------------|----------------|---------------|--------|----------------------------|--|------------------------|----------------------------|
|            |                |               |        |                            |  | Bootloader             | COM Mode (Active Firmware) |
| 0xE        | 0x0            | SystemCommand | W      | UIntegerT8 / (n.a)         | SSP 4.1.1:<br>Describes the PDI32.MSDC32_1 layout (one field of size 32bit, starting at offset 0x0). | x                      | x                          |

## 9.2.3 Identification

Table 55: Identification

| ISDU Index | ISDU Sub-Index | Name                   | Access | Datatype / (Default Value)                       | Further Info  | IO-Link Operation Mode   |                            |
|------------|----------------|------------------------|--------|--|---|--|----------------------------|
|            |                |                        |        |  |   | Bootloader   | COM Mode (Active Firmware) |
| 0x10       | 0x0            | VendorName             | R      | StringT48 / ("To be filled by Renesas customer") | Length of parameters may differ from specification in Reference 1 and Reference 2.<br><b>Note:</b> Modifiable via CCP.      | x  | x                          |
| 0x11       | 0x0            | VendorText             | R      | StringT48 / ("To be filled by Renesas customer") |   |  | x                          |
| 0x12       | 0x0            | ProductName            | R      | StringT32 / ("To be filled by Renesas customer") |   | x  | x                          |
| 0x13       | 0x0            | ProductID              | R      | StringT32 / ("To be filled")                     |   |  | x                          |
| 0x14       | 0x0            | ProductText            | R      | StringT48 / ("To be filled by Renesas customer") |   |  | x                          |
| 0x15       | 0x0            | SerialNumber           | R      | StringT16 / ("To be filled")                     |   |  | x                          |
| 0x16       | 0x0            | HardwareRevision       | R      | StringT16 / ("To be filled")                     |   | x  | x                          |
| 0x17       | 0x0            | FirmwareRevision       | R      | StringT32 / ([RCA version])                      |   | Contains ZSSC3286 TFW (RCA) release version. Length of parameter differs from specification in Reference 1 and Reference 2 |                            |
| 0x17       | 0x0            | FirmwareRevision       | R      | StringT32 / ([Bootloader version])               | Contains ZSSC3286 Bootloader release version. Length of parameter differs from specification in Reference 1 and Reference 2 | x  |                            |
| 0x18       | 0x0            | ApplicationSpecificTag | RW     | StringT32 / (****)                               |   |  | x                          |
| 0x19       | 0x0            | FunctionTag            | RW     | StringT32 / (****)                               |   |  | x                          |
| 0x1A       | 0x0            | LocationTag            | RW     | StringT32 / (****)                               |   |  | x                          |

## 9.2.4 Diagnosis

Table 56: Diagnosis

| ISDU Index | ISDU Sub-Index | Name                 | Access | Datatype / (Default Value) | Further Info | IO-Link Operation Mode |                            |
|------------|----------------|----------------------|--------|----------------------------|--------------|------------------------|----------------------------|
|            |                |                      |        |                            |              | Bootloader             | COM Mode (Active Firmware) |
| 0x20       | 0x0            | ErrorCount           | R      | UIntegerT16 / (0x0)        |              |                        | x                          |
| 0x24       | 0x0            | DeviceStatus         | R      | UIntegerT8 / (0x0)         |              |                        | x                          |
| 0x25       | 0x0            | DetailedDeviceStatus | R      | OctetStringT3 / (0x0)      |              |                        | x                          |

## 9.2.5 Process Data

**Note:** Table 57 column “ISDU Sub-Index” commands are not directly accessible. All parameter values within the ISDU Index are returned when sending command containing the ISDU Index with Sub-Index 0x0.

Table 57: Process Data

| ISDU Index | ISDU Sub-Index | Name              | Access | Datatype / (Default Value) | Further Info  | IO-Link Operation Mode |                            |
|------------|----------------|-------------------|--------|----------------------------|---|------------------------|----------------------------|
|            |                |                   |        |                            |   | Bootloader             | COM Mode (Active Firmware) |
| 0x28       | 0x1            | Measurement value | R      | IntegerT16 / (0x0)         |   |                        | x                          |
|            | 0x2            | Scale             | R      | IntegerT8 / (0x0)          |   |                        | x                          |
|            | 0x3            | SSC1.1            | R      | BooleanT / (0x0)           | SSC means Sensor Switching Channel in this occasion |                        | x                          |
|            | 0x4            | SSC1.2            | R      | BooleanT / (0x0)           |   |                        | x                          |

## 9.2.6 BLOB Transfer and Firmware Update

Table 58: BLOB Transfer

| ISDU Index | ISDU Sub-Index | Name    | Access | Datatype / (Default Value) | Further Info  | IO-Link Operation Mode |                            |
|------------|----------------|---------|--------|----------------------------|---|------------------------|----------------------------|
|            |                |         |        |                            |   | Bootloader             | COM Mode (Active Firmware) |
| 0x31       | 0x0            | BLOB_ID | R      | IntegerT16 / (n.a.)        | BLOB mechanism used for FW and CCP update<br>volatile values used for BLOB transfer | x                      |                            |
| 0x32       | 0x0            | BLOB_CH | RW     | variable / (n.a.)          |   | x                      |                            |

Table 59: Firmware Update

| ISDU Index | ISDU Sub-Index | Name           | Access | Datatype / (Default Value)   | Further Info  | IO-Link Operation Mode |                            |
|------------|----------------|----------------|--------|------------------------------|---|------------------------|----------------------------|
|            |                |                |        |                              |   | Bootloader             | COM Mode (Active Firmware) |
| 0x43BD     | 0x0            | FW-Password    | W      | StringT16 / (empty string)   | no password set by default<br><b>Note:</b> Modifiable via CCP |                        | x                          |
| 0x43BE     | 0x0            | HW ID Key      | R      | StringT16 / ("TO BE FILLED") | <b>Note:</b> Modifiable via CCP                               | x                      | x                          |
| 0x43BF     | 0x0            | BootmodeStatus | R      | UIntegerT8 / (0x0)           |   |                        | x                          |
| 0x43BF     | 0x0            | BootmodeStatus | R      | UIntegerT8 / (0x1)           |   | x                      |                            |



## 9.2.7 ISDU - Smart Sensor Profile (SSP)

**Note:** Table 60 column “ISDU Sub-Index” for ISDU Index 0x3B commands are not directly accessible. All parameter values within the ISDU Index are returned when sending command containing the ISDU Index with Sub-Index 0x0.

Table 60: Teach

| ISDU Index | ISDU Sub-Index | Name         | Access | Datatype / (Default Value) | Further Info | IO-Link Operation Mode |                            |
|------------|----------------|--------------|--------|----------------------------|--------------|------------------------|----------------------------|
|            |                |              |        |                            |              | Bootloader             | COM Mode (Active Firmware) |
| 0x3A       | 0x0            | TeachSelect  | RW     | UIntegerT8 / (0x1)         |              |                        | x                          |
| 0x3B       | 0x1            | State        | R      | UIntegerT4 / (0x0)         | Teach Result |                        | x                          |
|            | 0x2            | Flag SP1 TP1 | R      | BooleanT / (0x0)           |              |                        |                            |
|            | 0x3            | Flag SP1 TP2 | R      | BooleanT / (0x0)           |              |                        |                            |
|            | 0x4            | Flag SP2 TP1 | R      | BooleanT / (0x0)           |              |                        |                            |
|            | 0x5            | Flag SP2 TP2 | R      | BooleanT / (0x0)           |              |                        |                            |

Table 61: SSP 4.1.1: SSC1.1 Param (Sensor Switching Channel)

| ISDU Index | ISDU Sub-Index | Name       | Access | Datatype / (Default Value) | Further Info                             | IO-Link Operation Mode |                            |
|------------|----------------|------------|--------|----------------------------|--|------------------------|----------------------------|
|            |                |            |        |                            |  | Bootloader             | COM Mode (Active Firmware) |
| 0x3C       | 0x1            | Setpoint 1 | RW     | IntegerT32 / (0x0)         | switching channel deactivated by default |                        | x                          |
|            | 0x2            | Setpoint 2 | RW     | IntegerT32 / (0x0)         |  |                        |                            |
| 0x3D       | 0x1            | Logic      | RW     | UIntegerT8 / (0x0)         | SSC1.1Config (Sensor Switching Channel)  |                        | x                          |
|            | 0x2            | Mode       | RW     | UIntegerT8 / (0x0)         |  |                        |                            |
|            | 0x3            | Hyst       | RW     | IntegerT32 / (0x0)         |  |                        |                            |

Table 62: SSP 4.1.1: SSC1.2 Param (Sensor Switching Channel)

| ISDU Index | ISDU Sub-Index | Name       | Access | Datatype / (Default Value) | Further Info        | IO-Link Operation Mode |                            |
|------------|----------------|------------|--------|----------------------------|---------------------|------------------------|----------------------------|
|            |                |            |        |                            |                     | Bootloader             | COM Mode (Active Firmware) |
| 0x3E       | 0x1            | Setpoint 1 | RW     | IntegerT32 / (0x0)         | not used by default |                        | x                          |
|            | 0x2            | Setpoint 2 | RW     | IntegerT32 / (0x0)         |                     |                        |                            |
| 0x3F       | 0x1            | Logic      | RW     | UIntegerT8 / (0x0)         | SSC1.2Config        |                        | x                          |
|            | 0x2            | Mode       | RW     | UIntegerT8 / (0x0)         |                     |                        |                            |
|            | 0x3            | Hyst       | RW     | IntegerT32 / (0x0)         |                     |                        |                            |

**Note:** Table 63 column "ISDU Sub-Index" commands are not directly accessible. All parameter values within the ISDU Index are returned when sending command containing the ISDU Index with Sub-Index 0x0.

Table 63: SSP 4.1.1: MDC1Descr

| ISDU Index | ISDU Sub-Index | Name       | Access | Datatype / (Default Value) | Further Info   | IO-Link Operation Mode |                            |
|------------|----------------|------------|--------|----------------------------|--|------------------------|----------------------------|
|            |                |            |        |                            |  | Bootloader             | COM Mode (Active Firmware) |
| 0x4080     | 0x1            | LowerValue | R      | IntegerT32 / (0xFFFF8300)  | sign extended to 32bit<br><b>Note:</b> Modifiable via CCP.             |                        | x                          |
|            | 0x2            | UpperValue | R      | IntegerT32 / (0x7D00)      | <b>Note:</b> Modifiable via CCP.                                       |                        |                            |
|            | 0x3            | UnitCode   | R      | UIntegerT16 / (0d1130)     | corresponds to unit kPa by default<br><b>Note:</b> Modifiable via CCP. |                        |                            |
|            | 0x4            | Scale      | R      | IntegerT8 / (0d3)          |  |                        |                            |

## 9.2.8 ISDU - Vendor specific

Table 64: CCP Handling

| ISDU Index | ISDU Sub-Index | Name        | Access | Datatype / (Default Value) | Further Info   | IO-Link Operation Mode |                            |
|------------|----------------|-------------|--------|----------------------------|--|------------------------|----------------------------|
|            |                |             |        |                            |  | Bootloader             | COM Mode (Active Firmware) |
| 0x200      | 0x0            | CcpState    | R      | UIntegerT8 / (0x1)         | <ul style="list-style-type: none"> <li>• 0x0: CCP invalid</li> <li>• 0x1: CCP valid</li> </ul>   | x                      |                            |
| 0x201      | 0x0            | CcpPassword | W      | UIntegerT32 / (0xFFFFFFFF) | If password is other than 0xFFFFFFFF, it must be written before access to CCP is possible.<br>Shall not appear in IODD.<br><b>Note:</b> Modifiable via CCP | x                      | x                          |

**Table 65: HiddenCommand Interpreter**

| ISDU Index | ISDU Sub-Index | Name                    | Access | Datatype / (Default Value) | Further Info   | IO-Link Operation Mode |                            |
|------------|----------------|-------------------------|--------|----------------------------|--|------------------------|----------------------------|
|            |                |                         |        |                            |  | Bootloader             | COM Mode (Active Firmware) |
| 0x300      | 0x0            | Hidden Command          | W      | OctetStringT5 / n.a.       | HiddenCommand of variable length with payload. Shall not appear in IO-Link. See subsection 9.6 for details   |                        | x                          |
| 0x301      | 0x0            | Hidden Command Response | R      | OctetString T129 / (0x0)   | HiddenCommandResponse of variable length with Payload. Contains response to latest issued HiddenCommand. Shall not appear in IO-Link. See subsection 9.6 for details |                        | x                          |

### 9.3 I2C

ZSSC3286 supports I2C communication in Standard Mode, Fast Mode and Fast Mode+ on I2C SCL and I2C SDA pins. The I2C interface is listening to receive a telegram after system startup and whenever no IO-Link connection has been established.

I2C communication mode is selected and locked after I2C address match was passed and the first 8 bit of telegram data were received.

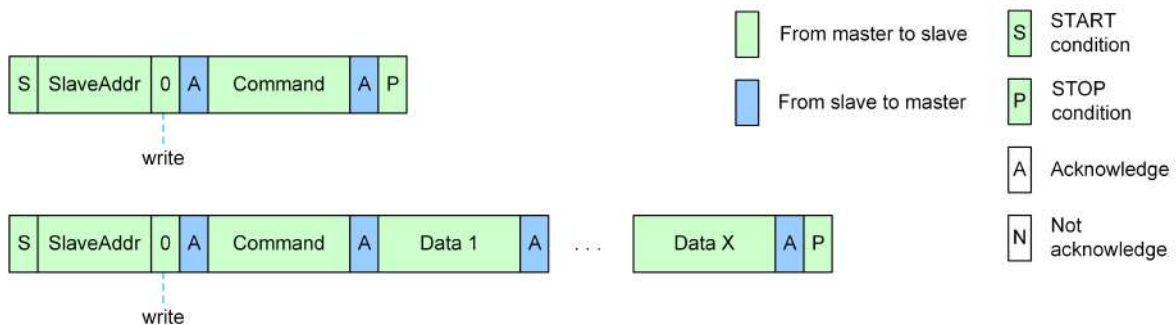
**Table 66: I2C Interface Parameter**

| Symbol                     | Parameter         | Conditions                | Minimum | Typical | Maximum | Units |
|----------------------------|-------------------|---------------------------|---------|---------|---------|-------|
| SlvAddr                    | I2C slave address | ZSSC3286 delivery default |         | 0x3C    |         |       |
| f <sub>SCL</sub> Interface | Clock             | I2C Mode                  | 0.1     |         | 1.0     | MHz   |
| D <sub>I2C</sub> Duty      | Cycle             |                           | 33      | –       | 50      | %     |

Timing and protocol details of the I2C communication in Standard Mode, Fast Mode, and Fast Mode+ are given in I2C-Bus Specification, Rev.6, UM10204. SCL clock stretching is not supported by ZSSC3286.

**Note:** When using third party tools for configuring the ZSSC3286 via I2C, it is recommended to wait at least 100ms after power up before sending I2C commands to ensure a stable communication.

In I2C Mode, each command request follows the structure shown in Figure 37. Only the number of data bytes needed by the command must be sent. See Table 70 for available commands.



**Figure 37: I2C Command Request**

Different available options for a response request are shown in Figure 38.

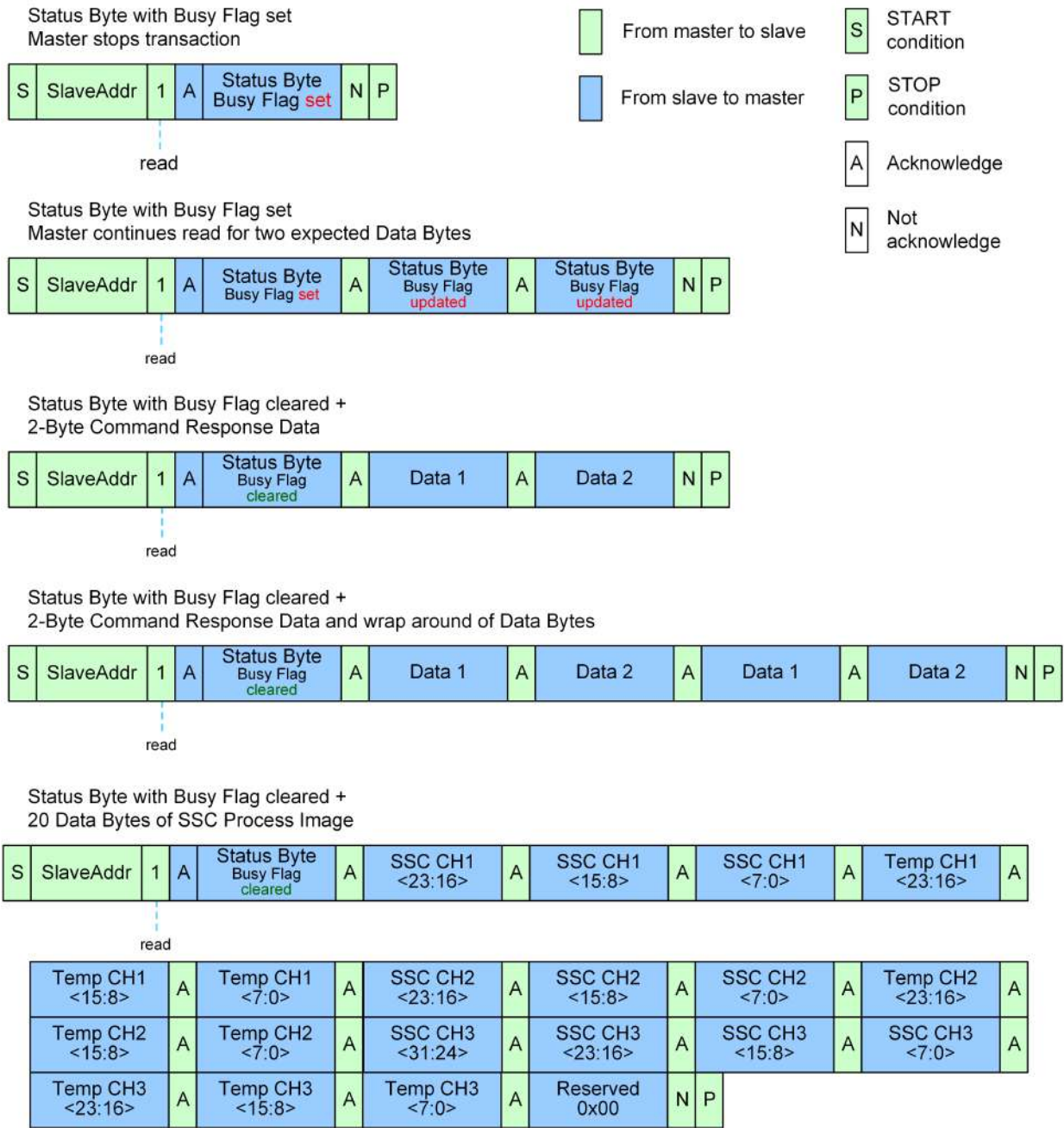


Figure 38: I2C Response Request

### 9.4 OWI

ZSSC3286 implements an OWI Master Interface solely used for configuring the RH4Z2501 IO-Link PHY. Register values are taken from PhyCfg1 Register. Refer to Memory Layout (section 12) for configuration options of the RH4Z2501. Refer to Application Notes (subsection 13.2 and subsection 13.3) for implementation recommendations.

The RH4Z2501 registers are configured with default values (Reference 3) in the default state of the ZSSC3286. If the IO-Link application requires different register settings for a successful connection, the configuration of the CCP register must be done in advance via I2C. Incorrect configuration may lead to inability to connect via IO-Link.

If the ZSSC3286 starts in bootloader after power up, for example if firmware update fails, the RH4Z2501 registers are not set by ZSSC3286 and contain default values. This may prevent an IO-Link connection if different values are needed. When switching from TFW (active firmware) to bootloader without a power cycle, the RH4Z2501 registers stay configured as set in CCP.

## 9.5 Command / Response Format

All commands follow the same command request (Table 67) format. Command response format will differ slightly for I2C and IO-Link communication according to (Table 68) and (Table 69). The number of data bytes which need to follow the command byte in the command request are returned after the Status Byte in command response, assuming the command execution was completed, is specific to the command code.

**Table 67: Command Request Format**

| Command       | Command Byte  |   |   |   |   |   |   |   | Data Bytes   |
|---------------|---------------|---|---|---|---|---|---|---|--------------|
|               | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |              |
| Valid Command | 8-bit command |   |   |   |   |   |   |   | [Data Bytes] |

**Table 68: I2C Command Response Format**

| Command   | Command Byte        |                 |           |   |  |              |                         |                         | Data Bytes   |
|---|---------------------|-----------------|-----------|---|--|--------------|-------------------------|-------------------------|--------------|
|   | 7                   | 6               | 5         | 4 | 3  | 2            | 1                       | 0                       |              |
| Previously received command in execution, response pending, New command not accepted, retry later | Telegram Error Flag | Power Supply OK | Busy Flag | 1 | SSC Mode<br>00: Command Mode<br>01: Cyclic Mode<br>10: Sleep Mode<br>11: Boot/Diagnosis Mode | Memory Error | Sensor Connection Fault | Saturation <sup>1</sup> | NONE         |
| Command successfully processed  |                     |                 |           | 0 |  |              |                         |                         | [Data Bytes] |

<sup>1</sup> Cleared before each command execution except for 0xA9 (Start Command Mode).

**Table 69: IO-Link Command Response Format**

| Command   | Command Byte        |   |   |   |   |   |  |   | Data Bytes   |
|---|---------------------|---|---|---|---|---|--|---|--------------|
|   | 7                   | 6 | 5 | 4 | 3 | 2 | 1  | 0 |              |
| Previously received command in execution, response pending, New command not accepted, retry later | Reserved (always 0) |   |   |   |   |   | Saturation (in commands 0xA7; 0xB2) <sup>1</sup> |   | NONE         |
| Command successfully processed  |                     |   |   |   |   |   |  |   | [Data Bytes] |

<sup>1</sup> Cleared before each command execution except for 0xA9 (Start Command Mode).

## 9.6 Command Interpreter

The availability of commands in Table 70 depends on the active main operating mode (Command or Cyclic Mode) and the current connection mode (I2C or IO-Link COM).

Commands available in IO-Link are called Hidden Commands. Except for commands related to FW Update functionality, the commands are for configuration and calibration purposes and are not required in final product application.

Some commands require an additional argument for successful command execution. If an argument error or missing argument appears, the current command is not executed. For IO-Link, a failure is indicated in the error response. For I2C, no error response is sent.

The commands available using IO-Link are called Hidden Commands. It is required to send commands via ISDU index 0x300 (sub-index 0x0) for writing and index 0x301 (sub-index 0x0) for reading the response. Reading the response requires sending an ISDU write command with the respective command code before sending an ISDU read command, see subsection 9.2.

Table 70: Command List

| Command Code (Byte)                                  | Return (after Status Byte)                                   | Description  | Command Available in |             |            |
|--|--|--|----------------------|-------------|------------|
|  |  |  | Command Mode         | Cyclic Mode | Bootloader |
| 0x82 followed by 0xXX + 0xWW                         | 0xWW × 4 bytes   | <b>Read configuration data in burst</b><br>Reads content of Configuration and Calibration Page (CCP) in burst mode:<br><ul style="list-style-type: none"> <li>0xXX selects the 32-bit word in CCP which is read first</li> <li>0xWW defines the number of words which is read from output memory</li> </ul> <b>Note:</b> Maximum supported 0xWW is 0x20<br><b>Note:</b> Before sending this command via IO-Link, set CCP Password must be sent via ISDU 0x201. | I2C<br>IO-Link       | IO-Link     |            |
| 0x83 followed by 0xXXYY + Data bytes (multiple of 4) | 1 byte (ACK / NACK)  | <b>Send CCP Update Chunk</b><br>Sends a data chunk during CCP Update<br><ul style="list-style-type: none"> <li>0xXXYY - chunk counter</li> <li>Data bytes - chunk fixed to size of 128 bytes</li> </ul> <b>Note:</b> Before sending this command via IO-Link, set CCP Password must be sent via ISDU 0x201.  |                      |             | I2C        |
| 0x84 followed by 0xXX + 0xWW                         | 0xWW × 4 bytes   | <b>Read device info data in burst</b><br>Reads device info data in burst mode :<br><ul style="list-style-type: none"> <li>0xXX selects the word in InfoPage which is read first</li> <li>0xWW defines the number of words which is read from output memory</li> </ul> <b>Note:</b> Maximum supported 0xXX is 0x1F<br><b>Note:</b> Maximum supported 0xWW is 0x20<br><b>Note:</b> If 0xXX + 0xWW is > 0x20, the command fails.                                  | I2C<br>IO-Link       | IO-Link     |            |
| 0x89   | 4 bytes (CCP version with PID)                               | <b>Read expected CCP Version</b>   | I2C<br>IO-Link       | IO-Link     |            |
| 0x8A   | 2 bytes  | <b>Read chip revision</b>  | I2C<br>IO-Link       | IO-Link     | I2C        |
| 0x8B   | 3 bytes (Bootloader Version)                                 | <b>Read Bootloader Version</b>   | I2C                  |             | I2C        |
| 0x8C   | n.a.<br>(Execution jumps directly to the FW update routines) | <b>Start Firmware Update</b><br>triggers Firmware update procedure   | I2C                  |             |            |
|  | 1 byte (ACK / NACK)  | <b>Send Firmware Update Chunk</b><br>Sends a data chunk during Firmware Update<br><ul style="list-style-type: none"> <li>0xXXYY - chunk counter</li> <li>Data bytes - chunk fixed to size of 128 bytes</li> </ul>  |                      |             | I2C        |
| 0x8D   | n.a.<br>(Device is immediately restarted)                    | <b>Restart the Device</b>  | I2C                  |             | I2C        |
| 0x8E   | 3 bytes (APP Firmware Version)                               | <b>Read Application Firmware Version</b>   | I2C                  |             |            |

Continued on next page

Table 70: Command List (Continued)

| Command Code (Byte)                      | Return (after Status Byte)        | Description   | Command Available in |                |            |
|--|-----------------------------------|---|----------------------|----------------|------------|
|  |                                   |   | Command Mode         | Cyclic Mode    | Bootloader |
| 0xA7 followed by 0xXX + 0xYY             | 20 bytes (Raw data)               | <b>Snapshot calibration all sensors<sup>1</sup></b><br>Returns unconditioned raw sensor and temperature data of all AFE channels that are activated in CCP. <ul style="list-style-type: none"> <li>0xXX minimum average count for AFE1 data</li> <li>0xYY minimum average count for AFE2 data</li> </ul> 0xXX and 0xYY must be in range 1 to 32 (=0x20).<br>The output data format is as follows: <ul style="list-style-type: none"> <li>Raw Data Bridge Sensor1 (24 bit)</li> <li>Raw Data Temperature Channel1 (24 bit)</li> <li>Raw Data Bridge Sensor2 (24 bit)</li> <li>Raw Data Temperature Channel2 (24 bit)</li> <li>0x00000000 (4 bytes 0x0) (32 bit)</li> <li>Raw Data Temperature Channel3 (24 bit)</li> <li>0x00 (1 byte 0x0) (8 bit)</li> </ul>  | I2C<br>IO-Link       |                |            |
| 0xA9                                     | n.a.                              | <b>Start Command Mode</b><br>Exit Cyclic Mode and transition to Command Mode  | I2C<br>IO-Link       | I2C<br>IO-Link |            |
| 0xAB                                     | n.a.                              | <b>Start Cyclic Mode</b><br>Enter Cyclic Mode based on configuration in Shadow RAM: continuous measurement cycles, SSC corrections, and automatic, continuous digital and/or analog output updates  | I2C<br>IO-Link       | IO-Link        |            |
| 0xB2 followed by data (0x0000 to 0xFFFF) | n.a.                              | <b>Update diagnosis status</b><br>Executes all activated sensor and system diagnosis checks   | IO-Link              |                |            |
| 0xB3                                     | n.a.                              | <b>Direct DAC Stimulus</b><br>Set the DAC output register with the data in the command and enable/output the respective analog signal through AOUT (according to the AOUT_setup)  | I2C                  |                |            |
| 0xB4 followed by 0x0X + 0xYY             | 2 bytes                           | <b>Self-diagnostic measure</b><br>for AFE1 and AFE2 Parameter 0x0X: <ul style="list-style-type: none"> <li>AFE1: 0x00</li> <li>AFE2: 0x01</li> <li>Parameter 0xYY</li> </ul> See description in Table 36  | IO-Link              |                |            |
| 0xB5 followed by 0xXX 0xYY 0xYY 0xYY     | n.a.                              | <b>Direct linear stimulus of analog output path</b><br>Stimulates the output path, linear relation between input data and pin output.<br>Parameter 0xXX - Output Selection: <ul style="list-style-type: none"> <li>0: reserved</li> <li>1: AOUT</li> <li>2: reserved</li> <li>3: reserved</li> </ul> Parameter 0xYYYYYY – Output Value: <ul style="list-style-type: none"> <li>24bit data value for output, unsigned integer (as SSC value format)</li> <li>assigned output is static (the output can be switched off by the RESN pin, POR, or a change in the main operating mode)</li> </ul> <b>Note:</b> The following workflow for the given command must be ensured: <ul style="list-style-type: none"> <li>Start Command Mode (0xA9)</li> <li>Set Direct linear stimulus of output path (0xB5)</li> <li>Reset the device</li> </ul> | I2C<br>IO-Link       |                |            |
| 0xB8                                     | 12 bytes (diagnostic result data) | <b>Read fault memory</b><br>Responds with the detailed fault-memory status (see section 7)  | IO-Link              | IO-Link        |            |

Continued on next page

Table 70: Command List (Continued)

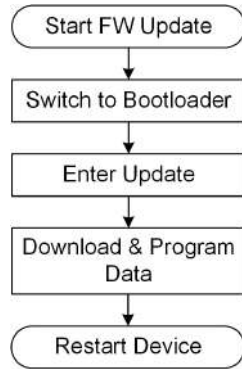
| Command Code (Byte) | Return (after Status Byte) | Description   | Command Available in |             |            |
|---------------------|----------------------------|---|----------------------|-------------|------------|
|                     |                            |   | Command Mode         | Cyclic Mode | Bootloader |
| 0xB9                | n.a.                       | <b>Reset fault memory</b><br>Resets the contents of the fault memory to 0x0   | IO-Link              | IO-Link     |            |
| 0xC0                | n.a.                       | <b>Story Factory Settings</b><br>Stores parameters for restoring via System Commands "BackToBox" and "ApplicationReset" | IO-Link              | IO-Link     |            |

- <sup>1</sup> These commands can be used to conduct a measurement without SSC conditioning, for example during the smart sensor calibration procedure. No digital correction is performed on the measurement result. The setup and configuration for the raw measurement is the content in the shadow registers that is automatically loaded from the Flash during power-on.



## 10 Firmware Update

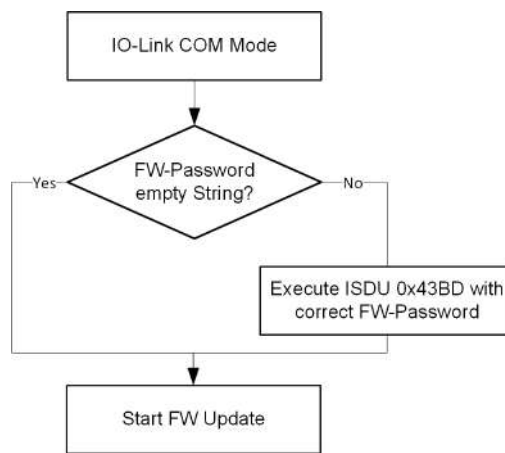
ZSSC3286 offers a firmware update function via IO-Link and via I2C interface for Renesas provided code (RCA code). IO-Link uses the BLOB transfer mechanism to download the IOLFW update file to the device. Figure 39 shows the high-level firmware update flow. After Initiating the firmware update, the device switches to Bootloader Mode. After the data is successfully transferred, the device is restarted.



**Figure 39: High-level Firmware Update Flow**

The Firmware Update access via IO-Link can be protected with the firmware password (FwPassword described in subsection 12.23), as shown in Figure 40. If the FW-Password is other than an empty String, it must be entered via ISDU Index 0x43BD in IO-Link COM Mode before starting Firmware Update. Otherwise, it prevents the device from entering bootloader and an error message is sent.

**Note:** The Firmware Update mechanism via I2C ignores the FW-Password protection.



**Figure 40: FW-Password Mechanism for Firmware Update**

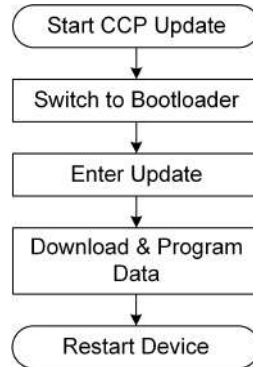
A firmware update is meant to be executed exclusively via the ZSSC3286 GUI and not by third party tools. Since a firmware update technically can be done via third party IO-Link tools, a firmware password should be set to prevent unauthorized firmware updates. It can be initiated at the FW UPDATE tab, where the respective new firmware file can be selected, and the update process can be triggered.

**Note:** Ensure a stable power supply during update. Power loss during update may cause corruption of the device.

## 11 CCP Update

ZSSC3286 offers a CCP update function via IO-Link and via I2C interface, triggered by the Write Memory button in the Renesas GUI. It uses similar update mechanisms to the Firmware Update described in section 10.

Figure 41 shows the high-level CCP update flow. After Initiating the CCP update, the device switches to Bootloader Mode. After the data is successfully transferred, the device is restarted.



**Figure 41: High-level CCP Update Flow**

The CCP Update access via IO-Link can be protected with the firmware password (See subsection 12.23 for *Fw-Password* and section 10 for firmware password mechanism) and the CCP password (CcpPassword see subsection 12.31.1), as shown in Figure 42.

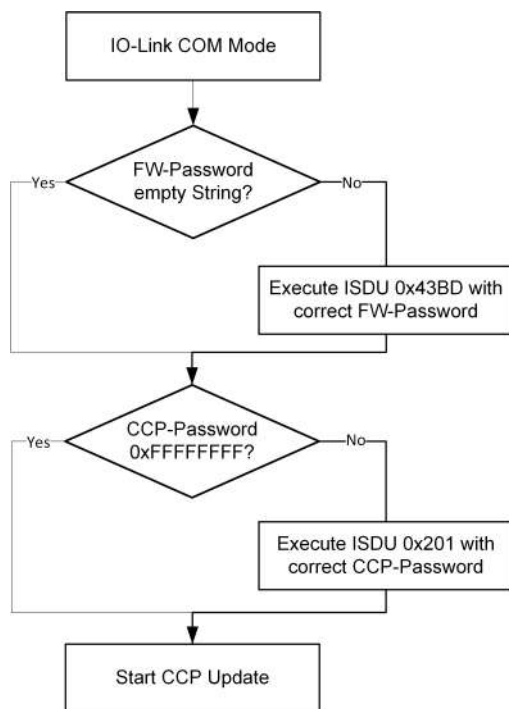
**Note:** If the CCP-Password is other than 0xFFFFFFFF, it must be entered via ISDU Index 0x201 in Bootloader before starting CCP update. Otherwise, it prevents the device from updating CCP via BLOB mechanism and an error message is sent.

Enter the passwords in the following order:

1. Enter FW-Password in IO-Link COM Mode
2. Enter Bootloader
3. Enter CCP-Password in Bootloader via IO-Link
4. Start CCP Update data transfer

**Note:** The CCP update mechanism via I2C ignores both the firmware password and the CCP password protection.

**Note:** The CCP-Password protects the device from reading CCP via IO-Link. The CCP-Password must be entered via ISDU 0x201 in IO-Link COM Mode prior to executing the Hidden Command 0x82 for CCP read.



**Figure 42: Password Mechanism for CCP Update**

Execute the CCP update exclusively via the ZSSC3286 GUI and not by third party tools and set the FW password and CCP password to prevent an unauthorized CCP update.

**Note:** Ensure a stable power supply during update. Power loss during update may cause corruption of the device.

## 12 Configuration and Calibration Page (CCP) Memory Map

This section describes the details and usage of single bitfields of CCP memory. The bitfields have two possible access attributes:

- **Reserved:** contains data that is set by Renesas and must not be changed from its default value.
- **Read/Write:** programmable with proper Read/Write access. By default all bitfields can be assumed as read and writeable. Thus an empty access information indicates an read and writeable bitfield.

### 12.1 IO-Link Settings

#### 12.1.1 0x02 – PhyCfg1

| Address : 0x02 |          | Register Name : PhyCfg1 |                            | Default: 0x004323E3   |
|----------------|----------|-------------------------|----------------------------|---|
| Bits           | Access   | Default                 | Field Name                 | Description   |
| 31:23          | Reserved | 0x0                     |                            | Reserved  |
| 22             |          | 0x1                     | PhyXcvrParam2.AutoRetryEn  | <b>Auto-retry enable</b> inside comCtrl2 register of RH4Z2501             |
| 21:20          |          | 0x0                     | PhyXcvrParam2.AutoRetryTim | <b>Auto-retry fixed off-time</b> inside comCtrl2 register of RH4Z2501     |
| 19:18          |          | 0x0                     | PhyXcvrParam2.BlankTim     | <b>Blanking time</b> inside comCtrl2 register of RH4Z2501                 |
| 17:16          |          | 0x3                     | PhyXcvrParam2.WuMode       | <b>Wake-up detection</b> inside comCtrl2 register of RH4Z2501             |
| 15:14          |          | 0x0                     | PhyXcvrParam1.DigFiltSel   | <b>Digital deglitch filter</b> inside comCtrl1 register of RH4Z2501       |
| 13             |          | 0x1                     | PhyXcvrParam1.AnaFiltEn    | <b>Analog (slow) deglitch filter</b> inside comCtrl1 register of RH4Z2501 |
| 12             |          | 0x0                     | PhyXcvrParam1.CqInv        | <b>C/Q Invert enable/disable</b> inside comCtrl1 register of RH4Z2501     |
| 11             |          | 0x0                     | PhyXcvrParam1.PullUpEn     | <b>Weak pull-up current source</b> inside comCtrl1 register of RH4Z2501   |
| 10             |          | 0x0                     | PhyXcvrParam1.PullDownEn   | <b>Weak pull-down current source</b> inside comCtrl1 register of RH4Z2501 |
| 9:8            |          | 0x3                     | PhyXcvrParam1.LsHsEn       | <b>C/Q driver mode</b> inside comCtrl1 register of RH4Z2501               |
| 7              |          | 0x1                     | PhyDriverParam.SlewRateEn  | <b>Enable slew rate</b> inside comParam register of RH4Z2501              |
| 6:4            |          | 0x6                     | PhyDriverParam.SlewRate    | <b>Value of slew rate</b> inside comParam register of RH4Z2501            |
| 3              | Reserved | 0x0                     |                            | Reserved  |
| 2:0            |          | 0x3                     | PhyDriverParam.CurrLim     | <b>Value of current limit</b> inside comParam register of RH4Z2501        |

#### 12.1.2 0x04 – IoIMisc

| Address : 0x04 |          | Register Name : IoIMisc |                         | Default: 0x00000006   |
|----------------|----------|-------------------------|-------------------------|---|
| Bits           | Access   | Default                 | Field Name              | Description   |
| 31:7           | Reserved | 0x0                     |                         | Reserved  |
| 6              |          | 0x0                     | AlarmInversion          | Inversion of ALARM signal<br>0x0 : Disabled<br>0x1 : Enabled  |
| 5              |          | 0x0                     | AlarmSwitchingSignalNum |   |
| 4:3            |          | 0x0                     | AlarmSwitchingChNum     | Sets the Measurement Data Channel (MDC) for the ALARM Signal (limited to MDC1 for SSP 4.1.1)                        |
| 2              |          | 0x1                     | LocatorEna              | IO-Link Locator Function Enable - transmitted in ISDU 0xD Subindex 0x7<br>0x0 : Disabled<br>0x1 : Enabled           |
| 1              |          | 0x1                     | SspDetectionMode        | IO-Link Detection Mode - transmitted in ISDU 0xD Subindex 0x6<br>0x0 : Object Detection<br>0x1 : Quantity Detection |
| 0              |          | 0x0                     | SioPdinFlag             | ALARM Function in SIO Mode<br>0x0 : Disabled<br>0x1 : Enabled   |

## 12.2 Basic AFE Setups

### 12.2.1 0x05 – AfeBaseCfgParam

| Address : 0x05 |        | Register Name : AfeBaseCfgParam |               | Default: 0x00000001  |
|----------------|--------|---------------------------------|---------------|--|
| Bits           | Access | Default                         | Field Name    | Description  |
| 31:24          |        | 0x0                             | AfeSyncStatus | AFE1 / AFE2 Synchronization<br>0x0 : Asynchronous measurement<br>0x1 : Synchronized measurement  |
| 23:16          |        | 0x0                             | Afe2SmConfig  | AFE2 Sequencer Configuration<br>0x0 : SM- and SM+<br>0x1 : SM+ and AUX_AZ<br>0x2 : SM+ only<br>0x3 : No Main Sensor-Bridge Measurement |
| 15:8           |        | 0x0                             | Afe1SmConfig  | AFE1 Sequencer Configuration<br>0x0 : SM- and SM+<br>0x1 : SM+ and AUX_AZ<br>0x2 : SM+ only<br>0x3 : No Main Sensor-Bridge Measurement |
| 7:0            |        | 0x1                             | AfeActive     | AFE Activation configuration<br>0x0 : None<br>0x1 : AFE1 only<br>0x2 : AFE2 only<br>0x3 : AFE1 and AFE2<br>0x7 : DualSpeed             |

### 12.2.2 0x06 – AfeBaseCfgParam.AfeDsCfg.Reg1

| Address : 0x06 |        | Register Name : AfeBaseCfgParam.AfeDsCfg.Reg1 |            | Default: 0x00000000     |
|----------------|--------|---|------------|-------------------------|
| Bits           | Access | Default                                       | Field Name | Description             |
| 31:24          |        | 0x0   | ConvCnt    | Feature not implemented |
| 23:0           |        | 0x0   | Thresh1    | Feature not implemented |

### 12.2.3 0x07 – AfeBaseCfgParam.AfeDsCfg.Reg2

| Address : 0x07 |          | Register Name : AfeBaseCfgParam.AfeDsCfg.Reg2 |            | Default: 0x00000000     |
|----------------|----------|---|------------|-------------------------|
| Bits           | Access   | Default                                       | Field Name | Description             |
| 31:24          | Reserved | 0x0   |            | Reserved                |
| 23:0           |          | 0x0   | Thresh2    | Feature not implemented |

## 12.3 Sensor Bridge

### 12.3.1 0x08 – Bm1Cfg1

| Address : 0x08 |          | Register Name : Bm1Cfg1 |               | Default: 0x04000655  |
|----------------|----------|-------------------------|---------------|--|
| Bits           | Access   | Default                 | Field Name    | Description  |
| 31             |          | 0x0                     | BmType        | Sensor Type<br>0x0 : Resistive Bridge<br>0x1 : Thermopile / Thermocouple   |
| 30             | Reserved | 0x0                     | BmTestDac     | AOUT DAC is used in diagnosis test   |
| 29             | Reserved | 0x0                     | BmTest        | PGA mux selects test pads  |
| 28:26          |          | 0x1                     | BmAdcMux      | ADC Input MUX Setting<br>0x0 : ADC inputs shorted to AGND<br>0x1 : ADC input connected to PGA<br>0x2 : ADC input connected to input (Gain = 1, PGA bypassed)   |
| 25:22          |          | 0x0                     | BmBrdgRtl     | Rtl resistor, applicable if BmBrdgType = 1<br>0x0 : Open      0x4 : 8000Ω      0x8 : 20000Ω<br>0x1 : 1333Ω      0x5 : 10000Ω      0x9 : 24000Ω<br>0x2 : 2000Ω      0x6 : 14000Ω      0xA : 28000Ω<br>0x3 : 4000Ω      0x7 : 18000Ω      0xB : 40000Ω |
| 21:18          |          | 0x0                     | BmBrdgRth     | Rth resistor, applicable if BmBrdgType = 1<br>0x0 : Open      0x4 : 8000Ω      0x8 : 20000Ω<br>0x1 : 1333Ω      0x5 : 10000Ω      0x9 : 24000Ω<br>0x2 : 2000Ω      0x6 : 14000Ω      0xA : 28000Ω<br>0x3 : 4000Ω      0x7 : 18000Ω      0xB : 40000Ω |
| 17:16          |          | 0x0                     | BmSetTime     | Bridge Settling Time before ADC conversion starts<br>0x0 : 20μs   0x1 : 40μs   0x2 : 60μs   0x3 : 80μs   |
| 15             |          | 0x0                     | BmBrdgType    | Bridge Supply via TOPx, BOTx<br>0x0 : Voltage Source<br>0x1 : Resistor or Current Source   |
| 14:12          |          | 0x0                     | BmAdcShift    | ADC Shift $V_{\text{Shift}} / V_{\text{fs}}$<br>0x0 : 0      0x2 : 0.250      0x4 : 0.500      0x6 : 0.750<br>0x1 : 0.125      0x3 : 0.375      0x5 : 0.625      0x7 : 0.875   |
| 11:8           |          | 0x6                     | BmAdcReso     | ADC Resolution<br>0x0 : 10 Bit   0x4 : 14 Bit   0x8 : 18 Bit   0xC : 22 Bit<br>0x1 : 11 Bit   0x5 : 15 Bit   0x9 : 19 Bit   0xD : 23 Bit<br>0x2 : 12 Bit   0x6 : 16 Bit   0xA : 20 Bit   0xE : 24 Bit<br>0x3 : 13 Bit   0x7 : 17 Bit   0xB : 21 Bit  |
| 7              |          | 0x0                     | BmPgaPolarity | PGA Polarity<br>0x0 : Positive<br>0x1 : Negative   |
| 6:4            |          | 0x5                     | BmPgaGain2    | PGA2 Gain<br>0x0 : 1.1   0x2 : 1.3   0x4 : 1.5   0x6 : 1.7<br>0x1 : 1.2   0x3 : 1.4   0x5 : 1.6   0x7 : 1.8  |
| 3:0            |          | 0x5                     | BmPgaGain1    | PGA1 Gain<br>0x0 : 1.2   0x3 : 5.97   0x6 : 29.6   0x9 : 76.6   0xC : 187<br>0x1 : 2   0x4 : 11.9   0x7 : 39.2   0xA : 112   0xD : 223<br>0x2 : 4   0x5 : 19.8   0x8 : 58.1   0xB : 143   0xE : 275  |

12.3.2 0x09 – Bm1Cfg2

| Address : 0x09 |          | Register Name : Bm1Cfg2 |              | Default: 0x00000210  |
|----------------|----------|-------------------------|--------------|--|
| Bits           | Access   | Default                 | Field Name   | Description  |
| 31:12          | Reserved | 0x0                     |              | Reserved   |
| 11:10          |          | 0x0                     | BmBias       | AFE Bias Current Setting<br>0x0 : normal operation<br>0x3 : reduced AFE bias current   |
| 9              |          | 0x1                     | BmAdcEnShift | ADC Shift & Gain ×2 Enable, activates <b>BmAdcShift</b> setting<br>0x0 : ADC Gain ×1, ADC Shift disabled<br>0x3 : ADC Gain ×2, ADC Shift enabled   |
| 8:5            |          | 0x0                     | BmBrdglBias  | Sensor Supply Current, applicable if BmBrdgType = 1<br>0x0 : Open/Off      0x4 : 40µA      0x8 : 200µA<br>0x1 : 5µA          0x5 : 80µA      0x9 : 500µA<br>0x2 : 10µA        0x6 : 100µA<br>0x3 : 20µA        0x7 : 160µA   |
| 4:0            |          | 0x10                    | BmPgaOffset  | PGA Offset Shift<br>0x1 : -1.9mV      0x10 : 0mV<br>0x2 : -3.8mV      0x11 : 1.9mV<br>0x3 : -5.6mV      0x12 : 3.8mV<br>0x4 : -7.5mV      0x13 : 5.6mV<br>0x5 : -9.4mV      0x14 : 7.5mV<br>0x6 : -11.3mV     0x15 : 9.4mV<br>0x7 : -13.1mV     0x16 : 11.3mV<br>0x8 : -15.0mV     0x17 : 13.1mV<br>0x9 : -16.9mV     0x18 : 15.0mV<br>0xA : -18.8mV     0x19 : 16.9mV<br>0xB : -20.6mV     0x1A : 18.8mV<br>0xC : -22.5mV     0x1B : 20.6mV<br>0xD : -24.4mV     0x1C : 22.5mV<br>0xE : -26.2mV     0x1D : 24.4mV<br>0xF : -28.1mV     0x1E : 26.2mV<br>0x1F : 28.1mV |

## 12.3.3 0x0A – Bm2Cfg1

| Address : 0x0A |          | Register Name : Bm2Cfg1 |               | Default: 0x04000656   |
|----------------|----------|-------------------------|---------------|---|
| Bits           | Access   | Default                 | Field Name    | Description   |
| 31             |          | 0x0                     | BmType        | Sensor Type<br>0x0 : Resistive Bridge<br>0x1 : Thermopile / Thermocouple  |
| 30             | Reserved | 0x0                     | BmTestDac     | AOUT DAC is used in diagnosis test  |
| 29             | Reserved | 0x0                     | BmTest        | PGA mux selects test pads   |
| 28:26          |          | 0x1                     | BmAdcMux      | ADC Input MUX Setting<br>0x0 : ADC inputs shorted to AGND<br>0x1 : ADC input connected to PGA<br>0x2 : ADC input connected to input (Gain = 1, PGA bypassed)  |
| 25:22          |          | 0x0                     | BmBrdgRtl     | Rtl resistor, applicable if BmBrdgType = 1<br>0x0 : Open   0x4 : 8000Ω   0x8 : 20000Ω<br>0x1 : 1333Ω   0x5 : 10000Ω   0x9 : 24000Ω<br>0x2 : 2000Ω   0x6 : 14000Ω   0xA : 28000Ω<br>0x3 : 4000Ω   0x7 : 18000Ω   0xB : 40000Ω                        |
| 21:18          |          | 0x0                     | BmBrdgRth     | Rth resistor, applicable if BmBrdgType = 1<br>0x0 : Open   0x4 : 8000Ω   0x8 : 20000Ω<br>0x1 : 1333Ω   0x5 : 10000Ω   0x9 : 24000Ω<br>0x2 : 2000Ω   0x6 : 14000Ω   0xA : 28000Ω<br>0x3 : 4000Ω   0x7 : 18000Ω   0xB : 40000Ω                        |
| 17:16          |          | 0x0                     | BmSetTime     | Bridge Settling Time before ADC conversion starts<br>0x0 : 20μs   0x1 : 40μs   0x2 : 60μs   0x3 : 80μs  |
| 15             |          | 0x0                     | BmBrdgType    | Bridge Supply via TOPx, BOTx<br>0x0 : Voltage Source<br>0x1 : Resistor or Current Source  |
| 14:12          |          | 0x0                     | BmAdcShift    | ADC Shift $V_{Shift} / V_{fs}$<br>0x0 : 0   0x2 : 0.250   0x4 : 0.500   0x6 : 0.750<br>0x1 : 0.125   0x3 : 0.375   0x5 : 0.625   0x7 : 0.875  |
| 11:8           |          | 0x6                     | BmAdcReso     | ADC Resolution<br>0x0 : 10 Bit   0x4 : 14 Bit   0x8 : 18 Bit   0xC : 22 Bit<br>0x1 : 11 Bit   0x5 : 15 Bit   0x9 : 19 Bit   0xD : 23 Bit<br>0x2 : 12 Bit   0x6 : 16 Bit   0xA : 20 Bit   0xE : 24 Bit<br>0x3 : 13 Bit   0x7 : 17 Bit   0xB : 21 Bit |
| 7              |          | 0x0                     | BmPgaPolarity | PGA Polarity<br>0x0 : Positive<br>0x1 : Negative  |
| 6:4            |          | 0x5                     | BmPgaGain2    | PGA2 Gain<br>0x0 : 1.1   0x2 : 1.3   0x4 : 1.5   0x6 : 1.7<br>0x1 : 1.2   0x3 : 1.4   0x5 : 1.6   0x7 : 1.8   |
| 3:0            |          | 0x6                     | BmPgaGain1    | PGA1 Gain<br>0x0 : 1.2   0x3 : 5.97   0x6 : 29.6   0x9 : 76.6   0xC : 187<br>0x1 : 2   0x4 : 11.9   0x7 : 39.2   0xA : 112   0xD : 223<br>0x2 : 4   0x5 : 19.8   0x8 : 58.1   0xB : 143   0xE : 275   |



## 12.3.4 0x0B – Bm2Cfg2

| Address : 0x0B |          | Register Name : Bm2Cfg2 |              | Default: 0x00000210  |
|----------------|----------|-------------------------|--------------|--|
| Bits           | Access   | Default                 | Field Name   | Description  |
| 31:12          | Reserved | 0x0                     |              | Reserved   |
| 11:10          |          | 0x0                     | BmBias       | AFE Bias Current Setting<br>0x0 : normal operation<br>0x3 : reduced AFE bias current   |
| 9              |          | 0x1                     | BmAdcEnShift | ADC Shift & Gain ×2 Enable, activates <b>BmAdcShift</b> setting<br>0x0 : ADC Gain ×1, ADC Shift disabled<br>0x3 : ADC Gain ×2, ADC Shift enabled   |
| 8:5            |          | 0x0                     | BmBrdglBias  | Sensor Supply Current, applicable if BmBrdgType = 1<br>0x0 : Open/Off      0x4 : 40μA      0x8 : 200μA<br>0x1 : 5μA          0x5 : 80μA      0x9 : 500μA<br>0x2 : 10μA        0x6 : 100μA<br>0x3 : 20μA        0x7 : 160μA   |
| 4:0            |          | 0x10                    | BmPgaOffset  | PGA Offset Shift<br>0x1 : -1.9mV      0x10 : 0mV<br>0x2 : -3.8mV      0x11 : 1.9mV<br>0x3 : -5.6mV      0x12 : 3.8mV<br>0x4 : -7.5mV      0x13 : 5.6mV<br>0x5 : -9.4mV      0x14 : 7.5mV<br>0x6 : -11.3mV     0x15 : 9.4mV<br>0x7 : -13.1mV     0x16 : 11.3mV<br>0x8 : -15.0mV     0x17 : 13.1mV<br>0x9 : -16.9mV     0x18 : 15.0mV<br>0xA : -18.8mV     0x19 : 16.9mV<br>0xB : -20.6mV     0x1A : 18.8mV<br>0xC : -22.5mV     0x1B : 20.6mV<br>0xD : -24.4mV     0x1C : 22.5mV<br>0xE : -26.2mV     0x1D : 24.4mV<br>0xF : -28.1mV     0x1E : 26.2mV<br>0x1F : 28.1mV |

## 12.4 External Temperature Sensor

### 12.4.1 0x0C – ExtTemp1Cfg1

| Address : 0x0C |          | Register Name : ExtTemp1Cfg1 |                    | Default: 0x0011C5F1  |
|----------------|----------|------------------------------|--------------------|--|
| Bits           | Access   | Default                      | Field Name         | Description  |
| 31:28          | Reserved | 0x0                          |                    | Reserved   |
| 27:24          |          | 0x0                          | ExtTempBrdgRtl     | Rtl resistor, applicable if BmBrdgType = 1<br>0x0 : Open      0x4 : 8000Ω      0x8 : 20000Ω<br>0x1 : 1333Ω    0x5 : 10000Ω    0x9 : 24000Ω<br>0x2 : 2000Ω    0x6 : 14000Ω    0xA : 28000Ω<br>0x3 : 4000Ω    0x7 : 18000Ω    0xB : 40000Ω   |
| 23:20          |          | 0x1                          | ExtTempBrdgRth     | Rth resistor, applicable if BmBrdgType = 1<br>0x0 : Open      0x4 : 8000Ω      0x8 : 20000Ω<br>0x1 : 1333Ω    0x5 : 10000Ω    0x9 : 24000Ω<br>0x2 : 2000Ω    0x6 : 14000Ω    0xA : 28000Ω<br>0x3 : 4000Ω    0x7 : 18000Ω    0xB : 40000Ω   |
| 19             |          | 0x0                          | ExtTempInput       | External Temperature Sensor Input MUX<br>0x0 : Input connected to PGA<br>0x1 : Input connected to ADC  |
| 18:15          |          | 0x3                          | ExtTempType        | External Temperature Type<br>0x0 : Reserved<br>0x1 : Diode/NTC/PTC sink mode, internal bias<br>0x2 : Diode/NTC/PTC, external bias<br>0x3 : Diode/NTC/PTC source mode, internal bias<br>0x4 : Reserved<br>0x5 : Bridge single ended, internal bias<br>0x6 : Bridge single ended, external bias<br>0x7 : Bridge differential |
| 14:12          |          | 0x4                          | ExtTempAdcShift    | ADC Shift $V_{Shift} / V_{fs}$<br>0x0 : 0      0x2 : 0.250    0x4 : 0.500    0x6 : 0.750<br>0x1 : 0.125    0x3 : 0.375    0x5 : 0.625    0x7 : 0.875   |
| 11:8           |          | 0x5                          | ExtTempAdcReso     | ADC Resolution<br>0x0 : 10 Bit    0x2 : 12 Bit    0x4 : 14 Bit<br>0x1 : 11 Bit    0x3 : 13 Bit    0x5 : 15 Bit   |
| 7              |          | 0x1                          | ExtTempPgaPolarity | PGA Polarity<br>0x0 : Positive<br>0x1 : Negative   |
| 6:4            |          | 0x7                          | ExtTempPgaGain2    | PGA2 Gain<br>0x0 : 1.1    0x2 : 1.3    0x4 : 1.5    0x6 : 1.7<br>0x1 : 1.2    0x3 : 1.4    0x5 : 1.6    0x7 : 1.8  |
| 3:0            |          | 0x1                          | ExtTempPgaGain1    | PGA1 Gain<br>0x0 : 1.2    0x3 : 5.97    0x6 : 29.6    0x9 : 76.6    0xC : 187<br>0x1 : 2      0x4 : 11.9    0x7 : 39.2    0xA : 112    0xD : 223<br>0x2 : 4      0x5 : 19.8    0x8 : 58.1    0xB : 143    0xE : 275  |

## 12.4.2 0x0D – ExtTemp1Cfg2

| Address : 0x0D |          | Register Name : ExtTemp1Cfg2 |                   | Default: 0x00000210   |
|----------------|----------|------------------------------|-------------------|---|
| Bits           | Access   | Default                      | Field Name        | Description   |
| 31:14          | Reserved | 0x0                          |                   | Reserved  |
| 13:12          |          | 0x0                          | ExtTempSetTime    | T1 Input Settling Time before ADC conversion starts<br>0x0 : 20μs   0x1 : 40μs   0x2 : 60μs   0x3 : 80μs  |
| 11:10          |          | 0x0                          | ExtTempBias       | AFE Bias Current Setting<br>0x0 : normal operation<br>0x3 : reduced AFE bias current  |
| 9              |          | 0x1                          | ExtTempAdcEnShift | ADC Shift & Gain ×2 Enable, activates <b>BmAdcShift</b> setting<br>0x0 : ADC Gain ×1, ADC Shift disabled<br>0x3 : ADC Gain ×2, ADC Shift enabled  |
| 8:5            |          | 0x0                          | ExtTempBrdglBias  | Sensor Supply Current, applicable if BmBrdgType = 1<br>0x0 : Open/Off   0x4 : 40μA   0x8 : 200μA<br>0x1 : 5μA   0x5 : 80μA   0x9 : 500μA<br>0x2 : 10μA   0x6 : 100μA<br>0x3 : 20μA   0x7 : 160μA  |
| 4:0            |          | 0x10                         | ExtTempPgaOffset  | PGA Offset Shift<br>0x1 : -1.9mV   0x10 : 0mV<br>0x2 : -3.8mV   0x11 : 1.9mV<br>0x3 : -5.6mV   0x12 : 3.8mV<br>0x4 : -7.5mV   0x13 : 5.6mV<br>0x5 : -9.4mV   0x14 : 7.5mV<br>0x6 : -11.3mV   0x15 : 9.4mV<br>0x7 : -13.1mV   0x16 : 11.3mV<br>0x8 : -15.0mV   0x17 : 13.1mV<br>0x9 : -16.9mV   0x18 : 15.0mV<br>0xA : -18.8mV   0x19 : 16.9mV<br>0xB : -20.6mV   0x1A : 18.8mV<br>0xC : -22.5mV   0x1B : 20.6mV<br>0xD : -24.4mV   0x1C : 22.5mV<br>0xE : -26.2mV   0x1D : 24.4mV<br>0xF : -28.1mV   0x1E : 26.2mV<br>0x1F : 28.1mV |

## 12.4.3 0x0E – ExtTemp2Cfg1

| Address : 0x0E |          | Register Name : ExtTemp2Cfg1 |                    | Default: 0x00118502  |
|----------------|----------|------------------------------|--------------------|--|
| Bits           | Access   | Default                      | Field Name         | Description  |
| 31:28          | Reserved | 0x0                          |                    | Reserved   |
| 27:24          |          | 0x0                          | ExtTempBrdgRtl     | Rtl resistor, applicable if BmBrdgType = 1<br>0x0 : Open      0x4 : 8000Ω      0x8 : 20000Ω<br>0x1 : 1333Ω      0x5 : 10000Ω      0x9 : 24000Ω<br>0x2 : 2000Ω      0x6 : 14000Ω      0xA : 28000Ω<br>0x3 : 4000Ω      0x7 : 18000Ω      0xB : 40000Ω   |
| 23:20          |          | 0x1                          | ExtTempBrdgRth     | Rth resistor, applicable if BmBrdgType = 1<br>0x0 : Open      0x4 : 8000Ω      0x8 : 20000Ω<br>0x1 : 1333Ω      0x5 : 10000Ω      0x9 : 24000Ω<br>0x2 : 2000Ω      0x6 : 14000Ω      0xA : 28000Ω<br>0x3 : 4000Ω      0x7 : 18000Ω      0xB : 40000Ω   |
| 19             |          | 0x0                          | ExtTempInput       | External Temperature Sensor Input MUX<br>0x0 : Input connected to PGA<br>0x1 : Input connected to ADC  |
| 18:15          |          | 0x3                          | ExtTempType        | External Temperature Type<br>0x0 : Reserved<br>0x1 : Diode/NTC/PTC sink mode, internal bias<br>0x2 : Diode/NTC/PTC, external bias<br>0x3 : Diode/NTC/PTC source mode, internal bias<br>0x4 : Reserved<br>0x5 : Bridge single ended, internal bias<br>0x6 : Bridge single ended, external bias<br>0x7 : Bridge differential |
| 14:12          |          | 0x0                          | ExtTempAdcShift    | ADC Shift $V_{Shift} / V_{fs}$<br>0x0 : 0      0x2 : 0.250      0x4 : 0.500      0x6 : 0.750<br>0x1 : 0.125      0x3 : 0.375      0x5 : 0.625      0x7 : 0.875   |
| 11:8           |          | 0x5                          | ExtTempAdcReso     | ADC Resolution<br>0x0 : 10 Bit      0x2 : 12 Bit      0x4 : 14 Bit<br>0x1 : 11 Bit      0x3 : 13 Bit      0x5 : 15 Bit   |
| 7              |          | 0x0                          | ExtTempPgaPolarity | PGA Polarity<br>0x0 : Positive<br>0x1 : Negative   |
| 6:4            |          | 0x0                          | ExtTempPgaGain2    | PGA2 Gain<br>0x0 : 1.1      0x2 : 1.3      0x4 : 1.5      0x6 : 1.7<br>0x1 : 1.2      0x3 : 1.4      0x5 : 1.6      0x7 : 1.8  |
| 3:0            |          | 0x2                          | ExtTempPgaGain1    | PGA1 Gain<br>0x0 : 1.2      0x3 : 5.97      0x6 : 29.6      0x9 : 76.6      0xC : 187<br>0x1 : 2      0x4 : 11.9      0x7 : 39.2      0xA : 112      0xD : 223<br>0x2 : 4      0x5 : 19.8      0x8 : 58.1      0xB : 143      0xE : 275  |

## 12.4.4 0x0F – ExtTemp2Cfg2

| Address : 0x0F |          | Register Name : ExtTemp2Cfg2 |                   | Default: 0x00000010   |
|----------------|----------|------------------------------|-------------------|---|
| Bits           | Access   | Default                      | Field Name        | Description   |
| 31:14          | Reserved | 0x0                          |                   | Reserved  |
| 13:12          |          | 0x0                          | ExtTempSetTime    | T1 Input Settling Time before ADC conversion starts<br>0x0 : 20μs   0x1 : 40μs   0x2 : 60μs   0x3 : 80μs  |
| 11:10          |          | 0x0                          | ExtTempBias       | AFE Bias Current Setting<br>0x0 : normal operation<br>0x3 : reduced AFE bias current  |
| 9              |          | 0x0                          | ExtTempAdcEnShift | ADC Shift & Gain ×2 Enable, activates <b>BmAdcShift</b> setting<br>0x0 : ADC Gain ×1, ADC Shift disabled<br>0x3 : ADC Gain ×2, ADC Shift enabled  |
| 8:5            |          | 0x0                          | ExtTempBrdglBias  | Sensor Supply Current, applicable if BmBrdgType = 1<br>0x0 : Open/Off   0x4 : 40μA   0x8 : 200μA<br>0x1 : 5μA   0x5 : 80μA   0x9 : 500μA<br>0x2 : 10μA   0x6 : 100μA<br>0x3 : 20μA   0x7 : 160μA  |
| 4:0            |          | 0x10                         | ExtTempPgaOffset  | PGA Offset Shift<br>0x1 : -1.9mV   0x10 : 0mV<br>0x2 : -3.8mV   0x11 : 1.9mV<br>0x3 : -5.6mV   0x12 : 3.8mV<br>0x4 : -7.5mV   0x13 : 5.6mV<br>0x5 : -9.4mV   0x14 : 7.5mV<br>0x6 : -11.3mV   0x15 : 9.4mV<br>0x7 : -13.1mV   0x16 : 11.3mV<br>0x8 : -15.0mV   0x17 : 13.1mV<br>0x9 : -16.9mV   0x18 : 15.0mV<br>0xA : -18.8mV   0x19 : 16.9mV<br>0xB : -20.6mV   0x1A : 18.8mV<br>0xC : -22.5mV   0x1B : 20.6mV<br>0xD : -24.4mV   0x1C : 22.5mV<br>0xE : -26.2mV   0x1D : 24.4mV<br>0xF : -28.1mV   0x1E : 26.2mV<br>0x1F : 28.1mV |

## 12.4.5 0x10 – ExtTemp3Cfg1

| Address : 0x10 |          | Register Name : ExtTemp3Cfg1 |                    | Default: 0x00118502  |
|----------------|----------|------------------------------|--------------------|--|
| Bits           | Access   | Default                      | Field Name         | Description  |
| 31:28          | Reserved | 0x0                          |                    | Reserved   |
| 27:24          |          | 0x0                          | ExtTempBrdgRtl     | Rtl resistor, applicable if BmBrdgType = 1<br>0x0 : Open      0x4 : 8000Ω      0x8 : 20000Ω<br>0x1 : 1333Ω    0x5 : 10000Ω    0x9 : 24000Ω<br>0x2 : 2000Ω    0x6 : 14000Ω    0xA : 28000Ω<br>0x3 : 4000Ω    0x7 : 18000Ω    0xB : 40000Ω   |
| 23:20          |          | 0x1                          | ExtTempBrdgRth     | Rth resistor, applicable if BmBrdgType = 1<br>0x0 : Open      0x4 : 8000Ω      0x8 : 20000Ω<br>0x1 : 1333Ω    0x5 : 10000Ω    0x9 : 24000Ω<br>0x2 : 2000Ω    0x6 : 14000Ω    0xA : 28000Ω<br>0x3 : 4000Ω    0x7 : 18000Ω    0xB : 40000Ω   |
| 19             |          | 0x0                          | ExtTempInput       | External Temperature Sensor Input MUX<br>0x0 : Input connected to PGA<br>0x1 : Input connected to ADC  |
| 18:15          |          | 0x3                          | ExtTempType        | External Temperature Type<br>0x0 : Reserved<br>0x1 : Diode/NTC/PTC sink mode, internal bias<br>0x2 : Diode/NTC/PTC, external bias<br>0x3 : Diode/NTC/PTC source mode, internal bias<br>0x4 : Reserved<br>0x5 : Bridge single ended, internal bias<br>0x6 : Bridge single ended, external bias<br>0x7 : Bridge differential |
| 14:12          |          | 0x0                          | ExtTempAdcShift    | ADC Shift $V_{Shift} / V_{fs}$<br>0x0 : 0      0x2 : 0.250    0x4 : 0.500    0x6 : 0.750<br>0x1 : 0.125    0x3 : 0.375    0x5 : 0.625    0x7 : 0.875   |
| 11:8           |          | 0x5                          | ExtTempAdcReso     | ADC Resolution<br>0x0 : 10 Bit    0x2 : 12 Bit    0x4 : 14 Bit<br>0x1 : 11 Bit    0x3 : 13 Bit    0x5 : 15 Bit   |
| 7              |          | 0x0                          | ExtTempPgaPolarity | PGA Polarity<br>0x0 : Positive<br>0x1 : Negative   |
| 6:4            |          | 0x0                          | ExtTempPgaGain2    | PGA2 Gain<br>0x0 : 1.1    0x2 : 1.3    0x4 : 1.5    0x6 : 1.7<br>0x1 : 1.2    0x3 : 1.4    0x5 : 1.6    0x7 : 1.8  |
| 3:0            |          | 0x2                          | ExtTempPgaGain1    | PGA1 Gain<br>0x0 : 1.2    0x3 : 5.97    0x6 : 29.6    0x9 : 76.6    0xC : 187<br>0x1 : 2      0x4 : 11.9    0x7 : 39.2    0xA : 112    0xD : 223<br>0x2 : 4      0x5 : 19.8    0x8 : 58.1    0xB : 143    0xE : 275  |

## 12.4.6 0x11 – ExtTemp3Cfg2

| Address : 0x11 |          | Register Name : ExtTemp3Cfg2 |                   | Default: 0x00000010  |
|----------------|----------|------------------------------|-------------------|--|
| Bits           | Access   | Default                      | Field Name        | Description  |
| 31:14          | Reserved | 0x0                          |                   | Reserved   |
| 13:12          |          | 0x0                          | ExtTempSetTime    | T1 Input Settling Time before ADC conversion starts<br>0x0 : 20μs   0x1 : 40μs   0x2 : 60μs   0x3 : 80μs   |
| 11:10          |          | 0x0                          | ExtTempBias       | AFE Bias Current Setting<br>0x0 : normal operation<br>0x3 : reduced AFE bias current   |
| 9              |          | 0x0                          | ExtTempAdcEnShift | ADC Shift & Gain ×2 Enable, activates <b>BmAdcShift</b> setting<br>0x0 : ADC Gain ×1, ADC Shift disabled<br>0x3 : ADC Gain ×2, ADC Shift enabled   |
| 8:5            |          | 0x0                          | ExtTempBrdglBias  | Sensor Supply Current, applicable if BmBrdgType = 1<br>0x0 : Open/Off   0x4 : 40μA   0x8 : 200μA<br>0x1 : 5μA   0x5 : 80μA   0x9 : 500μA<br>0x2 : 10μA   0x6 : 100μA<br>0x3 : 20μA   0x7 : 160μA   |
| 4:0            |          | 0x10                         | ExtTempPgaOffset  | PGA Offset Shift<br>0x1 : -1.9mV   0x10 : 0mV<br>0x2 : -3.8mV   0x11 : 1.9mV<br>0x3 : -5.6mV   0x12 : 3.8mV<br>0x4 : -7.5mV   0x13 : 5.6mV<br>0x5 : -9.4mV   0x14 : 7.5mV<br>0x6 : -11.3mV   0x15 : 9.4mV<br>0x7 : -13.1mV   0x16 : 11.3mV<br>0x8 : -15.0mV   0x17 : 13.1mV<br>0x9 : -16.9mV   0x18 : 15.0mV<br>0xA : -18.8mV   0x1A : 18.8mV<br>0xB : -20.6mV   0x1B : 20.6mV<br>0xC : -22.5mV   0x1C : 22.5mV<br>0xD : -24.4mV   0x1D : 24.4mV<br>0xE : -26.2mV   0x1E : 26.2mV<br>0xF : -28.1mV   0x1F : 28.1mV |

## 12.4.7 0x12 – AfeRegsAna.CmConfig[0]

| Address : 0x12 |        | Register Name : AfeRegsAna.CmConfig[0] |             | Default: 0x00000000 |
|----------------|--------|--|-------------|---------------------|
| Bits           | Access | Default                                | Field Name  | Description         |
| 31:0           |        | 0x0                                    | CmConfig[0] |                     |

## 12.4.8 0x13 – AfeRegsAna.CmConfig[1]

| Address : 0x13 |        | Register Name : AfeRegsAna.CmConfig[1] |             | Default: 0x00000000 |
|----------------|--------|--|-------------|---------------------|
| Bits           | Access | Default                                | Field Name  | Description         |
| 31:0           |        | 0x0                                    | CmConfig[1] |                     |

## 12.4.9 0x14 – AfeRegsAna.CmConfig[2]

| Address : 0x14 |        | Register Name : AfeRegsAna.CmConfig[2] |             | Default: 0x00000000 |
|----------------|--------|--|-------------|---------------------|
| Bits           | Access | Default                                | Field Name  | Description         |
| 31:0           |        | 0x0                                    | CmConfig[2] |                     |

## 12.5 PTAT Sensor

### 12.5.1 0x15 – PtatCfg1

| Address : 0x15 |          | Register Name : PtatCfg1 |             | Default: 0x0000F533   |
|----------------|----------|--------------------------|-------------|---|
| Bits           | Access   | Default                  | Field Name  | Description   |
| 31:18          | Reserved | 0x0                      |             | Reserved  |
| 17:15          |          | 0x1                      | AdcMux      | ADC Input MUX Setting<br>0x1 : ADC input connected to PGA <sup>1</sup>  |
| 14:12          |          | 0x7                      | AdcShift    | ADC Shift $V_{Shift} / V_{fs}$<br>0x0 : 0    0x2 : 0.250    0x4 : 0.500    0x6 : 0.750<br>0x1 : 0.125    0x3 : 0.375    0x5 : 0.625    0x7 : 0.875 <sup>1</sup>   |
| 11:8           |          | 0x5                      | AdcReso     | ADC Resolution<br>0x0 : 10 Bit    0x2 : 12 Bit    0x4 : 14 Bit<br>0x1 : 11 Bit    0x3 : 13 Bit    0x5 : 15 Bit  |
| 7              |          | 0x0                      | PgaPolarity | PGA Polarity<br>0x0 : Positive <sup>1</sup><br>0x1 : Negative   |
| 6:4            |          | 0x3                      | PgaGain2    | PGA2 Gain<br>0x0 : 1.1    0x2 : 1.3    0x4 : 1.5    0x6 : 1.7<br>0x1 : 1.2    0x3 : 1.4 <sup>1</sup> 0x5 : 1.6    0x7 : 1.8   |
| 3:0            |          | 0x3                      | PgaGain1    | PGA1 Gain<br>0x0 : 1.2    0x3 : 5.97 <sup>1</sup> 0x6 : 29.6    0x9 : 76.6    0xC : 187<br>0x1 : 2    0x4 : 11.9    0x7 : 39.2    0xA : 112    0xD : 223<br>0x2 : 4    0x5 : 19.8    0x8 : 58.1    0xB : 143    0xE : 275 |

<sup>1</sup> Renesas recommended

### 12.5.2 0x16 – PtatCfg2

| Address : 0x16 |          | Register Name : PtatCfg2 |            | Default: 0x00000030   |
|----------------|----------|--------------------------|------------|---|
| Bits           | Access   | Default                  | Field Name | Description   |
| 31:8           | Reserved | 0x0                      |            | Reserved  |
| 7:6            |          | 0x0                      | Bias       | AFE Bias Current Setting<br>0x0 : normal operation<br>0x3 : reduced AFE bias current  |
| 5              |          | 0x1                      | AdcEnShift | ADC Shift & Gain ×2 Enable, activates <b>AdcShift</b> setting<br>0x0 : ADC Gain ×1, ADC Shift disabled<br>0x3 : ADC Gain ×2, ADC Shift enabled <sup>1</sup>   |
| 4:0            |          | 0x10                     | PgaOffset  | PGA Offset Shift<br>0x1 : -1.9mV    0x10 : 0mV <sup>1</sup><br>0x2 : -3.8mV    0x11 : 1.9mV<br>0x3 : -5.6mV    0x12 : 3.8mV<br>0x4 : -7.5mV    0x13 : 5.6mV<br>0x5 : -9.4mV    0x14 : 7.5mV<br>0x6 : -11.3mV    0x15 : 9.4mV<br>0x7 : -13.1mV    0x16 : 11.3mV<br>0x8 : -15.0mV    0x17 : 13.1mV<br>0x9 : -16.9mV    0x18 : 15.0mV<br>0xA : -18.8mV    0x19 : 16.9mV<br>0xB : -20.6mV    0x1A : 18.8mV<br>0xC : -22.5mV    0x1B : 20.6mV<br>0xD : -24.4mV    0x1C : 22.5mV<br>0xE : -26.2mV    0x1D : 24.4mV<br>0xF : -28.1mV    0x1E : 26.2mV<br>0x1F : 28.1mV |

<sup>1</sup> Renesas recommended



## 12.6 AFE Sequencer

### 12.6.1 0x17 – Afe1MeasCfg1

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

| Address : 0x17 |        | Register Name : Afe1MeasCfg1 |                | Default: 0x01020036  |
|----------------|--------|------------------------------|----------------|--|
| Bits           | Access | Default                      | Field Name     | Description  |
| 31             |        | 0x0                          | BurstModeSlot8 | AFE DMA Burst Mode Data Transfer after Slot_x<br>0x0 : Disabled<br>0x1 : Enabled       |
| 30             |        | 0x0                          | BurstModeSlot7 |  |
| 29             |        | 0x0                          | BurstModeSlot6 |  |
| 28             |        | 0x0                          | BurstModeSlot5 |  |
| 27             |        | 0x0                          | BurstModeSlot4 |  |
| 26             |        | 0x0                          | BurstModeSlot3 |  |
| 25             |        | 0x0                          | BurstModeSlot2 |  |
| 24             |        | 0x1                          | BurstModeSlot1 |  |
| 23             |        | 0x0                          | EoclrqSlot8    | End of Conversion Interrupt after Slot_x<br>0x0 : Disabled<br>0x1 : Enabled            |
| 22             |        | 0x0                          | EoclrqSlot7    |  |
| 21             |        | 0x0                          | EoclrqSlot6    |  |
| 20             |        | 0x0                          | EoclrqSlot5    |  |
| 19             |        | 0x0                          | EoclrqSlot4    |  |
| 18             |        | 0x0                          | EoclrqSlot3    |  |
| 17             |        | 0x1                          | EoclrqSlot2    |  |
| 16             |        | 0x0                          | EoclrqSlot1    |  |
| 15:14          |        | 0x0                          | MeasTypeSlot8  | AFE Measurement Type for Slot_x<br>0x0 : None<br>0x1 : SM-<br>0x2 : SM+<br>0x3 : AUX_i |
| 13:12          |        | 0x0                          | MeasTypeSlot7  |  |
| 11:10          |        | 0x0                          | MeasTypeSlot6  |  |
| 9:8            |        | 0x0                          | MeasTypeSlot5  |  |
| 7:6            |        | 0x0                          | MeasTypeSlot4  |  |
| 5:4            |        | 0x3                          | MeasTypeSlot3  |  |
| 3:2            |        | 0x1                          | MeasTypeSlot2  |  |
| 1:0            |        | 0x2                          | MeasTypeSlot1  |  |

### 12.6.2 0x18 – Afe1MeasCfg2

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

| Address : 0x18 |          | Register Name : Afe1MeasCfg2 |               | Default: 0x00000013  |
|----------------|----------|------------------------------|---------------|--|
| Bits           | Access   | Default                      | Field Name    | Description  |
| 31:24          | Reserved | 0x0                          |               | Reserved   |
| 23:8           |          | 0x0                          | AuxMaxTime    | Maximum length of AUX_i measurement slots within a sequence<br>0x0000 ... 0xFFFF AFE clock cycles<br>The parameter is calculated based on the relevant timing setups of all active AUX_i measurements to secure all AUX_i measurements have the same duration. This is mainly required for synchronized AFE operation. |
| 7:6            |          | 0x0                          | AuxInsertRate | Insertion Rate of an AUX_i measurement in „Accelerated main measurement“ setup<br>0x0 : Disabled<br>0x1 : Every 2nd<br>0x2 : Every 4th<br>0x3 : Every 8th  |
| 5:4            |          | 0x1                          | CyclicMode    | Sequencer Run Mode<br>0x0 : Single measurement<br>0x1 : Continuous cyclic measurement<br>0x2 : Discontinuous cyclic measurement, started by trigger  |
| 3:0            |          | 0x3                          | NrOfSlots     | Number of active measurement slots<br>0x0 ... 0x8 selectable   |

## 12.6.3 0x19 – Afe1MeasCfg3

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

| Address : 0x19 |          | Register Name : Afe1MeasCfg3 |                     | Default: 0x00000018   |
|----------------|----------|------------------------------|---------------------|---|
| Bits           | Access   | Default                      | Field Name          | Description   |
| 31             | Reserved | 0x0                          | AuxMeasEnable0Aux32 | Activation of Auxiliary measurements<br>Bit 0 : Auto-zero (AZ) measurement on Sensor Bridge<br>Bit 1 : PTAT Sensor S-<br>Bit 2 : PTAT Sensor S+<br>Bit 3 : T1 Sensor S-<br>Bit 4 : T1 Sensor S+<br>Bit 5 : T1 Sensor, check short to top<br>Bit 6 : T1 Sensor, check short to bottom<br>Bit 7 : T1 Sensor, check open<br>Bit 8 : T2 Sensor S-<br>Bit 9 : T2 Sensor S+<br>Bit 10 : T2 Sensor, check short to top<br>Bit 11 : T2 Sensor, check short to bottom<br>Bit 12 : T2 Sensor, check open<br>Bit 13 : T3 Sensor S-<br>Bit 14 : T3 Sensor S+<br>Bit 15 : T3 Sensor, check short to top<br>Bit 16 : T3 Sensor, check short to bottom<br>Bit 17 : T3 Sensor, check open<br>Bit 18 : AFE gain diagnosis S+<br>Bit 19 : AFE gain diagnosis S-<br>Bit 22 : AFE offset diagnosis<br>Bit 27 : Bridge Sensor connection check, INP or INN open<br>Bit 28 : Bridge Sensor connection check, INP and INN shorted<br><br>All other bits reserved<br><br>Bit Value Meaning<br>0 : Aux measurement Skipped<br>1 : Aux measurement Executed |
| 30             | Reserved | 0x0                          | AuxMeasEnable0Aux31 |   |
| 29             | Reserved | 0x0                          | AuxMeasEnable0Aux30 |   |
| 28             |          | 0x0                          | AuxMeasEnable0Aux29 |   |
| 27             |          | 0x0                          | AuxMeasEnable0Aux28 |   |
| 26             |          | 0x0                          | AuxMeasEnable0Aux27 |   |
| 25             |          | 0x0                          | AuxMeasEnable0Aux26 |   |
| 24             |          | 0x0                          | AuxMeasEnable0Aux25 |   |
| 23             |          | 0x0                          | AuxMeasEnable0Aux24 |   |
| 22             |          | 0x0                          | AuxMeasEnable0Aux23 |   |
| 21             |          | 0x0                          | AuxMeasEnable0Aux22 |   |
| 20             |          | 0x0                          | AuxMeasEnable0Aux21 |   |
| 19             |          | 0x0                          | AuxMeasEnable0Aux20 |   |
| 18             |          | 0x0                          | AuxMeasEnable0Aux19 |   |
| 17             |          | 0x0                          | AuxMeasEnable0Aux18 |   |
| 16             |          | 0x0                          | AuxMeasEnable0Aux17 |   |
| 15             |          | 0x0                          | AuxMeasEnable0Aux16 |   |
| 14             |          | 0x0                          | AuxMeasEnable0Aux15 |   |
| 13             |          | 0x0                          | AuxMeasEnable0Aux14 |   |
| 12             |          | 0x0                          | AuxMeasEnable0Aux13 |   |
| 11             |          | 0x0                          | AuxMeasEnable0Aux12 |   |
| 10             |          | 0x0                          | AuxMeasEnable0Aux11 |   |
| 9              |          | 0x0                          | AuxMeasEnable0Aux10 |   |
| 8              |          | 0x0                          | AuxMeasEnable0Aux9  |   |
| 7              |          | 0x0                          | AuxMeasEnable0Aux8  |   |
| 6              |          | 0x0                          | AuxMeasEnable0Aux7  |   |
| 5              |          | 0x0                          | AuxMeasEnable0Aux6  |   |
| 4              |          | 0x1                          | AuxMeasEnable0Aux5  |   |
| 3              |          | 0x1                          | AuxMeasEnable0Aux4  |   |
| 2              |          | 0x0                          | AuxMeasEnable0Aux3  |   |
| 1              |          | 0x0                          | AuxMeasEnable0Aux2  |   |
| 0              |          | 0x0                          | AuxMeasEnable0Aux1  |   |

## 12.6.4 0x1A – Afe1MeasCfg4

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

| Address : 0x1A |          | Register Name : Afe1MeasCfg4 |                     | Default: 0x00400000  |
|----------------|----------|------------------------------|---------------------|--|
| Bits           | Access   | Default                      | Field Name          | Description  |
| 31:25          | Reserved | 0x0                          |                     | Reserved   |
| 24             |          | 0x0                          | SensBufDepth        | Bridge Sensor data buffer depth in SRAM<br>0x0 : data buffer depth 1<br>0x1 : data buffer depth 8  |
| 23             |          | 0x0                          | IrqEnableEoauxaz    | End of AZ Measurement<br>0x0 : IRQ disabled<br>0x1 : IRQ enabled   |
| 22             |          | 0x1                          | IrqEnableEoauxseq   | End of Aux Sequence<br>0x0 : IRQ disabled<br>0x1 : IRQ enabled   |
| 21             |          | 0x0                          | IrqEnableEoauxins   | End of Inserted AUX Measurement<br>0x0 : IRQ disabled<br>0x1 : IRQ enabled   |
| 20:5           |          | 0x0                          | IdleTime            | In continuous cyclic measurement mode idle times up to 10ms can be asserted between two sequences.<br>IdleTime represents a number of AFE clocks – 4MHz by default |
| 4              | Reserved | 0x0                          | AuxMeasEnable1Aux37 | Enable CVC diagnosis leak_2 S+   |
| 3              | Reserved | 0x0                          | AuxMeasEnable1Aux36 | Enable CVC diagnosis leak_2 S-   |
| 2              | Reserved | 0x0                          | AuxMeasEnable1Aux35 | Enable CVC diagnosis leak_1 S+   |
| 1              | Reserved | 0x0                          | AuxMeasEnable1Aux34 | Enable CVC diagnosis leak_1 S-   |
| 0              | Reserved | 0x0                          | AuxMeasEnable1Aux33 | Enable sensor leakage check P  |

### 12.6.5 0x1B – Afe2MeasCfg1

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

| Address : 0x1B |        | Register Name : Afe2MeasCfg1 |                | Default: 0x01020036  |
|----------------|--------|------------------------------|----------------|--|
| Bits           | Access | Default                      | Field Name     | Description  |
| 31             |        | 0x0                          | BurstModeSlot8 | AFE DMA Burst Mode Data Transfer after Slot_x<br>0x0 : Disabled<br>0x1 : Enabled       |
| 30             |        | 0x0                          | BurstModeSlot7 |  |
| 29             |        | 0x0                          | BurstModeSlot6 |  |
| 28             |        | 0x0                          | BurstModeSlot5 |  |
| 27             |        | 0x0                          | BurstModeSlot4 |  |
| 26             |        | 0x0                          | BurstModeSlot3 |  |
| 25             |        | 0x0                          | BurstModeSlot2 |  |
| 24             |        | 0x1                          | BurstModeSlot1 |  |
| 23             |        | 0x0                          | EocIrqSlot8    | End of Conversion Interrupt after Slot_x<br>0x0 : Disabled<br>0x1 : Enabled            |
| 22             |        | 0x0                          | EocIrqSlot7    |  |
| 21             |        | 0x0                          | EocIrqSlot6    |  |
| 20             |        | 0x0                          | EocIrqSlot5    |  |
| 19             |        | 0x0                          | EocIrqSlot4    |  |
| 18             |        | 0x0                          | EocIrqSlot3    |  |
| 17             |        | 0x1                          | EocIrqSlot2    |  |
| 16             |        | 0x0                          | EocIrqSlot1    |  |
| 15:14          |        | 0x0                          | MeasTypeSlot8  | AFE Measurement Type for Slot_x<br>0x0 : None<br>0x1 : SM-<br>0x2 : SM+<br>0x3 : AUX_i |
| 13:12          |        | 0x0                          | MeasTypeSlot7  |  |
| 11:10          |        | 0x0                          | MeasTypeSlot6  |  |
| 9:8            |        | 0x0                          | MeasTypeSlot5  |  |
| 7:6            |        | 0x0                          | MeasTypeSlot4  |  |
| 5:4            |        | 0x3                          | MeasTypeSlot3  |  |
| 3:2            |        | 0x1                          | MeasTypeSlot2  |  |
| 1:0            |        | 0x2                          | MeasTypeSlot1  |  |

### 12.6.6 0x1C – Afe2MeasCfg2

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

| Address : 0x1C |          | Register Name : Afe2MeasCfg2 |               | Default: 0x00000013  |
|----------------|----------|------------------------------|---------------|--|
| Bits           | Access   | Default                      | Field Name    | Description  |
| 31:24          | Reserved | 0x0                          |               | Reserved   |
| 23:8           |          | 0x0                          | AuxMaxTime    | Maximum length of AUX_i measurement slots within a sequence<br>0x0000 ... 0xFFFF AFE clock cycles<br>The parameter is calculated based on the relevant timing setups of all active AUX_i measurements to secure all AUX_i measurements have the same duration. This is mainly required for synchronized AFE operation. |
| 7:6            |          | 0x0                          | AuxInsertRate | Insertion Rate of an AUX_i measurement in „Accelerated main measurement“ setup<br>0x0 : Disabled<br>0x1 : Every 2nd<br>0x2 : Every 4th<br>0x3 : Every 8th  |
| 5:4            |          | 0x1                          | CyclicMode    | Sequencer Run Mode<br>0x0 : Single measurement<br>0x1 : Continuous cyclic measurement<br>0x2 : Discontinuous cyclic measurement, started by trigger  |
| 3:0            |          | 0x3                          | NrOfSlots     | Number of active measurement slots<br>0x0 ... 0x8 selectable   |

## 12.6.7 0x1D – Afe2MeasCfg3

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

| Address : 0x1D |          | Register Name : Afe2MeasCfg3 |                     | Default: 0x00000000   |
|----------------|----------|------------------------------|---------------------|---|
| Bits           | Access   | Default                      | Field Name          | Description   |
| 31             | Reserved | 0x0                          | AuxMeasEnable0Aux32 | Activation of Auxiliary measurements<br>Bit 0 : Auto-zero (AZ) measurement on Sensor Bridge<br>Bit 1 : PTAT Sensor S-<br>Bit 2 : PTAT Sensor S+<br>Bit 3 : T1 Sensor S-<br>Bit 4 : T1 Sensor S+<br>Bit 5 : T1 Sensor, check short to top<br>Bit 6 : T1 Sensor, check short to bottom<br>Bit 7 : T1 Sensor, check open<br>Bit 8 : T2 Sensor S-<br>Bit 9 : T2 Sensor S+<br>Bit 10 : T2 Sensor, check short to top<br>Bit 11 : T2 Sensor, check short to bottom<br>Bit 12 : T2 Sensor, check open<br>Bit 13 : T3 Sensor S-<br>Bit 14 : T3 Sensor S+<br>Bit 15 : T3 Sensor, check short to top<br>Bit 16 : T3 Sensor, check short to bottom<br>Bit 17 : T3 Sensor, check open<br>Bit 18 : AFE gain diagnosis S+<br>Bit 19 : AFE gain diagnosis S-<br>Bit 22 : AFE offset diagnosis<br>Bit 27 : Bridge Sensor connection check, INP or INN open<br>Bit 28 : Bridge Sensor connection check, INP and INN shorted<br><br>All other bits reserved<br><br>Bit Value Meaning<br>0 : Aux measurement Skipped<br>1 : Aux measurement Executed |
| 30             | Reserved | 0x0                          | AuxMeasEnable0Aux31 |   |
| 29             | Reserved | 0x0                          | AuxMeasEnable0Aux30 |   |
| 28             |          | 0x0                          | AuxMeasEnable0Aux29 |   |
| 27             |          | 0x0                          | AuxMeasEnable0Aux28 |   |
| 26             |          | 0x0                          | AuxMeasEnable0Aux27 |   |
| 25             |          | 0x0                          | AuxMeasEnable0Aux26 |   |
| 24             |          | 0x0                          | AuxMeasEnable0Aux25 |   |
| 23             |          | 0x0                          | AuxMeasEnable0Aux24 |   |
| 22             |          | 0x0                          | AuxMeasEnable0Aux23 |   |
| 21             |          | 0x0                          | AuxMeasEnable0Aux22 |   |
| 20             |          | 0x0                          | AuxMeasEnable0Aux21 |   |
| 19             |          | 0x0                          | AuxMeasEnable0Aux20 |   |
| 18             |          | 0x0                          | AuxMeasEnable0Aux19 |   |
| 17             |          | 0x0                          | AuxMeasEnable0Aux18 |   |
| 16             |          | 0x0                          | AuxMeasEnable0Aux17 |   |
| 15             |          | 0x0                          | AuxMeasEnable0Aux16 |   |
| 14             |          | 0x0                          | AuxMeasEnable0Aux15 |   |
| 13             |          | 0x0                          | AuxMeasEnable0Aux14 |   |
| 12             |          | 0x0                          | AuxMeasEnable0Aux13 |   |
| 11             |          | 0x0                          | AuxMeasEnable0Aux12 |   |
| 10             |          | 0x0                          | AuxMeasEnable0Aux11 |   |
| 9              |          | 0x0                          | AuxMeasEnable0Aux10 |   |
| 8              |          | 0x0                          | AuxMeasEnable0Aux9  |   |
| 7              |          | 0x0                          | AuxMeasEnable0Aux8  |   |
| 6              |          | 0x0                          | AuxMeasEnable0Aux7  |   |
| 5              |          | 0x0                          | AuxMeasEnable0Aux6  |   |
| 4              |          | 0x0                          | AuxMeasEnable0Aux5  |   |
| 3              |          | 0x0                          | AuxMeasEnable0Aux4  |   |
| 2              |          | 0x0                          | AuxMeasEnable0Aux3  |   |
| 1              |          | 0x0                          | AuxMeasEnable0Aux2  |   |
| 0              |          | 0x0                          | AuxMeasEnable0Aux1  |   |

## 12.6.8 0x1E – Afe2MeasCfg4

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

| Address : 0x1E |          | Register Name : Afe2MeasCfg4 |                     | Default: 0x00000000  |
|----------------|----------|------------------------------|---------------------|--|
| Bits           | Access   | Default                      | Field Name          | Description  |
| 31:25          | Reserved | 0x0                          |                     | Reserved   |
| 24             |          | 0x0                          | SensBufDepth        | Bridge Sensor data buffer depth in SRAM<br>0x0 : data buffer depth 1<br>0x1 : data buffer depth 8  |
| 23             |          | 0x0                          | IrqEnableEoauxaz    | End of AZ Measurement<br>0x0 : IRQ disabled<br>0x1 : IRQ enabled   |
| 22             |          | 0x0                          | IrqEnableEoauxseq   | End of Aux Sequence<br>0x0 : IRQ disabled<br>0x1 : IRQ enabled   |
| 21             |          | 0x0                          | IrqEnableEoauxins   | End of Inserted AUX Measurement<br>0x0 : IRQ disabled<br>0x1 : IRQ enabled   |
| 20:5           |          | 0x0                          | IdleTime            | In continuous cyclic measurement mode idle times up to 10ms can be asserted between two sequences.<br>IdleTime represents a number of AFE clocks – 4MHz by default |
| 4              | Reserved | 0x0                          | AuxMeasEnable1Aux37 | Enable CVC diagnosis leak_2 S+   |
| 3              | Reserved | 0x0                          | AuxMeasEnable1Aux36 | Enable CVC diagnosis leak_2 S-   |
| 2              | Reserved | 0x0                          | AuxMeasEnable1Aux35 | Enable CVC diagnosis leak_1 S+   |
| 1              | Reserved | 0x0                          | AuxMeasEnable1Aux34 | Enable CVC diagnosis leak_1 S-   |
| 0              | Reserved | 0x0                          | AuxMeasEnable1Aux33 | Enable sensor leakage check P  |

## 12.7 Diagnosis

### 12.7.1 0x1F – DiagSen.DiagCfg

| Address : 0x1F |          | Register Name : DiagSen.DiagCfg |                      | Default: 0x00000000   |
|----------------|----------|---------------------------------|----------------------|---|
| Bits           | Access   | Default                         | Field Name           | Description   |
| 31:17          | Reserved | 0x0                             |                      | Reserved  |
| 16:15          |          | 0x0                             | Extt3Range           | Reference for Temp Sensor open check on T3<br>0x0 : 2MΩ<br>0x1 : 0.5MΩ<br>0x3 : 0.1MΩ                     |
| 14             |          | 0x0                             | Extt3Pt100           | Reference for temperature sensor short measurement on T3<br>0x0 : RT_SHORT < 500Ω<br>0x1 : RT_SHORT < 10Ω |
| 13             | Reserved | 0x0                             |                      | Reserved  |
| 12:11          |          | 0x0                             | Extt2Range           | Reference for Temp Sensor open check on T2<br>0x0 : 2MΩ<br>0x1 : 0.5MΩ<br>0x3 : 0.1MΩ                     |
| 10             |          | 0x0                             | Extt2Pt100           | Reference for temperature sensor short measurement on T2<br>0x0 : RT_SHORT < 500Ω<br>0x1 : RT_SHORT < 10Ω |
| 9              | Reserved | 0x0                             |                      | Reserved  |
| 8:7            |          | 0x0                             | Extt1Range           | Reference for Temp Sensor open check on T1<br>0x0 : 2MΩ<br>0x1 : 0.5MΩ<br>0x3 : 0.1MΩ                     |
| 6              |          | 0x0                             | Extt1Pt100           | Reference for temperature sensor short measurement on T1<br>0x0 : RT_SHORT < 500Ω<br>0x1 : RT_SHORT < 10Ω |
| 5:4            |          | 0x0                             | Afe2GainChkResDacVal | Resistive Diagnosis DAC value at AFE2<br>0x0 : 2mV<br>0x1 : 10mV<br>0x2 : 100mV<br>0x3 : 200mV            |
| 3              |          | 0x0                             | Afe2GainChkResDacEn  | Resistive Diagnosis DAC activation at AFE2<br>0x0 : Disabled<br>0x1 : Enabled                             |
| 2:1            |          | 0x0                             | Afe1GainChkResDacVal | Resistive Diagnosis DAC value at AFE1<br>0x0 : 2mV<br>0x1 : 10mV<br>0x2 : 100mV<br>0x3 : 200mV            |
| 0              |          | 0x0                             | Afe1GainChkResDacEn  | Resistive Diagnosis DAC activation at AFE1<br>0x0 : Disabled<br>0x1 : Enabled                             |

### 12.7.2 0x20 – DiagSen.Range[0].Inp

| Address : 0x20 |        | Register Name : DiagSen.Range[0].Inp |            | Default: 0x00000000 |
|----------------|--------|--------------------------------------|------------|---------------------|
| Bits           | Access | Default                              | Field Name | Description         |
| 31:16          |        | 0x0                                  | Max        |                     |
| 15:0           |        | 0x0                                  | Min        |                     |

### 12.7.3 0x21 – DiagSen.Range[0].Inn

| Address : 0x21 |        | Register Name : DiagSen.Range[0].Inn |            | Default: 0x00000000 |
|----------------|--------|--------------------------------------|------------|---------------------|
| Bits           | Access | Default                              | Field Name | Description         |
| 31:16          |        | 0x0                                  | Max        |                     |
| 15:0           |        | 0x0                                  | Min        |                     |

## 12.7.4 0x22 – DiagSen.Range[1].Inp

| Address : 0x22 |        | Register Name : DiagSen.Range[1].Inp |            | Default: 0x00000000 |
|----------------|--------|--------------------------------------|------------|---------------------|
| Bits           | Access | Default                              | Field Name | Description         |
| 31:16          |        | 0x0                                  | Max        |                     |
| 15:0           |        | 0x0                                  | Min        |                     |

## 12.7.5 0x23 – DiagSen.Range[1].Inn

| Address : 0x23 |        | Register Name : DiagSen.Range[1].Inn |            | Default: 0x00000000 |
|----------------|--------|--------------------------------------|------------|---------------------|
| Bits           | Access | Default                              | Field Name | Description         |
| 31:16          |        | 0x0                                  | Max        |                     |
| 15:0           |        | 0x0                                  | Min        |                     |

## 12.7.6 0x24 – DiagSen.GainChk[0]

| Address : 0x24 |        | Register Name : DiagSen.GainChk[0] |            | Default: 0x00000000  |
|----------------|--------|------------------------------------|------------|--|
| Bits           | Access | Default                            | Field Name | Description  |
| 31:16          |        | 0x0                                | TolVal     | Gain Tolerance Value for Gain Drift Diagnosis<br>A tolerance value in ADC counts for acceptable gain drift over lifetime shall be stored in this register<br>A gain failure is signaled after the Gain Drift Check if the determined AFE Gain Value is either $< (\text{RefVal} - \text{TolVal})$ or $> (\text{RefVal} + \text{TolVal})$ |
| 15:0           |        | 0x0                                | RefVal     | Gain Reference Value for Gain Drift Diagnosis<br>During sensor calibration an initial AFE Gain Check measurement with a properly defined AFExGainCheckResDacVal setting must be done and the obtained RAW output value shall be stored in this register for later reference.   |

## 12.7.7 0x25 – DiagSen.GainChk[1]

| Address : 0x25 |        | Register Name : DiagSen.GainChk[1] |            | Default: 0x00000000 |
|----------------|--------|------------------------------------|------------|---------------------|
| Bits           | Access | Default                            | Field Name | Description         |
| 31:16          |        | 0x0                                | TolVal     |                     |
| 15:0           |        | 0x0                                | RefVal     |                     |

## 12.7.8 0x26 – DiagSen.OfstChk[0]

| Address : 0x26 |        | Register Name : DiagSen.OfstChk[0] |            | Default: 0x00000000 |
|----------------|--------|------------------------------------|------------|---------------------|
| Bits           | Access | Default                            | Field Name | Description         |
| 31:16          |        | 0x0                                | TolVal     |                     |
| 15:0           |        | 0x0                                | RefVal     |                     |

## 12.7.9 0x27 – DiagSen.OfstChk[1]

| Address : 0x27 |        | Register Name : DiagSen.OfstChk[1] |            | Default: 0x00000000 |
|----------------|--------|------------------------------------|------------|---------------------|
| Bits           | Access | Default                            | Field Name | Description         |
| 31:16          |        | 0x0                                | TolVal     |                     |
| 15:0           |        | 0x0                                | RefVal     |                     |



## 12.8 Temperature Channel Mapping

### 12.8.1 0x28 – TempMapChId

| Address : 0x28 |          | Register Name : TempMapChId |            | Default: 0x00000002  |
|----------------|----------|-----------------------------|------------|--|
| Bits           | Access   | Default                     | Field Name | Description  |
| 31:9           | Reserved | 0x0                         |            | Reserved   |
| 8:6            |          | 0x0                         | Tch3       | Temperature Sensor Source for Temperature Channels 1, 2, 3<br>0x0 : None<br>0x1 : PTAT<br>0x2 : T1<br>0x3 : T2<br>0x4 : T3 |
| 5:3            |          | 0x0                         | Tch2       |  |
| 2:0            |          | 0x2                         | Tch1       |  |

## 12.9 SSC Algorithm Selection

### 12.9.1 0x29 – MathSbrAlgoSel

| Address : 0x29 |          | Register Name : MathSbrAlgoSel |            | Default: 0x00000011   |
|----------------|----------|--------------------------------|------------|---|
| Bits           | Access   | Default                        | Field Name | Description   |
| 31:12          | Reserved | 0x0                            |            | Reserved  |
| 11             |          | 0x0                            | TlcChOrder | Third Logic Channel Operand Order<br>0x0 : CH1 op CH2<br>0x1 : CH2 op CH1                         |
| 10:8           |          | 0x0                            | TlcOp      | Third Logic Channel Operation<br>0x0 : Subtraction<br>0x1 : Division<br>0x2 : Ratio               |
| 7:4            |          | 0x1                            | Sensor2    | SSC Algorithm for Bridge Sensors 1 & 2<br>0x0 : None<br>0x1 : SOT Parabolic<br>0x2 : SOT S-Shaped |
| 3:0            |          | 0x1                            | Sensor1    |   |

## 12.10 Analog Output (AOUT)

### 12.10.1 0x2A – AoutSelParam

| Address : 0x2A |          | Register Name : AoutSelParam |              | Default: 0x00000001   |
|----------------|----------|------------------------------|--------------|---|
| Bits           | Access   | Default                      | Field Name   | Description   |
| 31:6           | Reserved | 0x0                          |              | Reserved  |
| 5:3            |          | 0x0                          | AoutModSel   | Analog Output Driver Mode<br>0x0 : Disabled<br>0x1 : Absolute Voltage Output 0-10V<br>0x2 : Absolute Voltage Output 0-5V<br>0x3 : Absolute V 0-1V<br>0x4 : Ratiometric Voltage Output<br>0x5 : 2-Wire Current Loop<br>0x6 : 3-Wire Current Loop<br>0x7 : Auto-Detect Current Loop |
| 2:0            |          | 0x1                          | SelAfeForDac | Source Signal for Analog Output<br>0x0 : None<br>0x1 : Bridge Sensor Channel 1<br>0x2 : Bridge Sensor Channel 2<br>0x3 : Third Logic Channel<br>0x4 : Temperature Channel 1<br>0x5 : Temperature Channel 2<br>0x6 : Temperature Channel 3   |

## 12.10.2 0x2B – AoutRegCtrl

| Address : 0x2B |          | Register Name : AoutRegCtrl |                   | Default: 0x0000001A  |
|----------------|----------|-----------------------------|-------------------|--|
| Bits           | Access   | Default                     | Field Name        | Description  |
| 31:11          | Reserved | 0x0                         |                   | Reserved   |
| 10:9           |          | 0x0                         | AoutVddnLoad      | VDDN Charge Pump Load Current<br>0x0 : 0.5mA      0x2 : 3mA<br>0x1 : 1mA        0x3 : 5mA                        |
| 8              |          | 0x0                         | AoutVddnEn        | VDDN Charge Pump for Negative Supply<br>0x0 : Disabled<br>0x1 : Enabled  |
| 7              |          | 0x0                         | AoutOffsetCompOff | Analog Output Offset Compensation<br>0x0 : Disabled<br>0x1 : Enabled   |
| 6:5            |          | 0x0                         | AoutCurrLim       | Analog Driver Output Current Limitation<br>0x0 : 6mA        0x2 : 18mA<br>0x1 : 12mA       0x3 : 25mA            |
| 4              |          | 0x1                         | AoutFeedBackEn    | Analog Driver Feedback<br>0x0 : External<br>0x1 : Internal   |
| 3              |          | 0x1                         | AoutHighPowEn     | Analog Driver Output Power<br>0x0 : Low Power<br>0x1 : High Power  |
| 2:1            |          | 0x1                         | AoutMode          | Analog Output Mode<br>0x0 : Current Loop 5V-RDAC<br>0x1 : VOUT 5V<br>0x2 : VOUT 1V<br>0x3 : Current Loop 1V-RDAC |
| 0              |          | 0x0                         | AoutEn            | Analog Output Activation<br>0x0 : Disabled<br>0x1 : Enabled  |

## 12.10.3 0x2C – AoutRegDiag

| Address : 0x2C |          | Register Name : AoutRegDiag |                  | Default: 0x00000000  |
|----------------|----------|-----------------------------|------------------|--|
| Bits           | Access   | Default                     | Field Name       | Description  |
| 31:4           | Reserved | 0x0                         |                  | Reserved   |
| 3              |          | 0x0                         | AoutDiagVddaEn   | VDDA Diagnosis if VDDA regulator for AOUT is turned on<br>0x0 : Disabled<br>0x1 : Enabled                                    |
| 2:1            |          | 0x0                         | AoutDiagOutValue | Analog Output Mode<br>0x0 : $V_{AOUT} = VSS$ 0x2 : $V_{AOUT} = 96\%VDD$<br>0x1 : $V_{AOUT} = 5\% VDD$ 0x3 : $V_{AOUT} = VDD$ |
| 0              |          | 0x0                         | AoutDiagOutEn    | Diagnosis Level Output at AOUT<br>0x0 : Normal Operation Mode<br>0x1 : Diagnosis Output Mode                                 |

## 12.10.4 0x2D – AoutCI3Coeff

| Address : 0x2D |        | Register Name : AoutCI3Coeff |            | Default: 0x00000000  |
|----------------|--------|------------------------------|------------|--|
| Bits           | Access | Default                      | Field Name | Description  |
| 31:16          |        | 0x0                          | CIDelta    | 2-Wire Current Loop Calibration Coefficient CL2_Delta<br>16-bit Value  |
| 15:0           |        | 0x0                          | CIOffset   | 2-Wire Current Loop Calibration Coefficient CL2_Offset<br>16-bit Value |

## 12.11 System Startup

### 12.11.1 0x2E – StartupParamCfg

| Address : 0x2E |          | Register Name : StartupParamCfg |             | Default: 0x00000001  |
|----------------|----------|---------------------------------|-------------|--|
| Bits           | Access   | Default                         | Field Name  | Description  |
| 31:1           | Reserved | 0x0                             |             | Reserved   |
| 0              |          | 0x1                             | StartupMode | System Startup Mode<br>0x0 : Cyclic Mode<br>0x1 : Command Mode |

## 12.12 IIR Filter

### 12.12.1 0x2F – IirFiltCoeffReg

| Address : 0x2F |          | Register Name : IirFiltCoeffReg |               | Default: 0x00000000                  |
|----------------|----------|---------------------------------|---------------|--------------------------------------|
| Bits           | Access   | Default                         | Field Name    | Description                          |
| 31:30          | Reserved | 0x0                             |               | Reserved                             |
| 29:27          |          | 0x0                             | FiltTemp3Diff | IIR Diff Value Temperature Channel 3 |
| 26:24          |          | 0x0                             | FiltTemp3Avg  | IIR Avg Value Temperature Channel 3  |
| 23:21          |          | 0x0                             | FiltTemp2Diff | IIR Diff Value Temperature Channel 2 |
| 20:18          |          | 0x0                             | FiltTemp2Avg  | IIR Avg Value Temperature Channel 2  |
| 17:15          |          | 0x0                             | FiltTemp1Diff | IIR Diff Value Temperature Channel 1 |
| 14:12          |          | 0x0                             | FiltTemp1Avg  | IIR Avg Value Temperature Channel 1  |
| 11:9           |          | 0x0                             | FiltSbr2Diff  | IIR Diff Value Sensor Bridge 2       |
| 8:6            |          | 0x0                             | FiltSbr2Avg   | IIR Avg Value Sensor Bridge 2        |
| 5:3            |          | 0x0                             | FiltSbr1Diff  | IIR Diff Value Sensor Bridge 1       |
| 2:0            |          | 0x0                             | FiltSbr1Avg   | IIR Avg Value Sensor Bridge 1        |

## 12.13 General AFE Configuration

### 12.13.1 0x30 – AfeConfig

| Address : 0x30 |          | Register Name : AfeConfig |                   | Default: 0x00000000   |
|----------------|----------|---------------------------|-------------------|---|
| Bits           | Access   | Default                   | Field Name        | Description   |
| 31             |          | 0x0                       | CLMode            | AFE Operation Mode for 2-Wire Current Loop application<br>0x0 : Disabled<br>0x1 : Enabled                         |
| 30:26          | Reserved | 0x0                       | AfeMisc           | Reserved  |
| 25             |          | 0x0                       | Afe2LowSpeed      | AFE2 clock speed with respect to AFE1<br>0x0 : Normal (equal) Speed<br>0x1 : Quarter Speed                        |
| 24             | Reserved | 0x0                       | CM2En             | Reserved  |
| 23             | Reserved | 0x0                       | CM1En             | Reserved  |
| 22             |          | 0x0                       | Vdda3Brownout     | AOUT Vdda Brownout Diagnosis<br>0x0 : Disabled<br>0x1 : Enabled   |
| 21             |          | 0x0                       | Vdda2Brownout     | AFE2 Vdda Brownout Diagnosis<br>0x0 : Disabled<br>0x1 : Enabled   |
| 20             |          | 0x0                       | Vdda1Brownout     | AFE1 Vdda Brownout Diagnosis<br>0x0 : Disabled<br>0x1 : Enabled   |
| 19             | Reserved | 0x0                       | CMDitheringEnable | Reserved  |
| 18             | Reserved | 0x0                       | CMNoiseInt1       | Reserved  |
| 17             |          | 0x0                       | TNoiseInt1        | ADC 10 $\mu$ V Noise Reduction<br>0x0 : Disabled<br>0x1 : Enabled   |
| 16             |          | 0x0                       | ExtTemp3NoiseInt1 |   |
| 15             |          | 0x0                       | ExtTemp2NoiseInt1 |   |
| 14             |          | 0x0                       | ExtTemp1NoiseInt1 |   |
| 13             |          | 0x0                       | BM2NoiseInt1      |   |
| 12             |          | 0x0                       | BM1NoiseInt1      |   |
| 11:10          |          | 0x0                       | TChpMode          | PGA Chopper Mode PTAT Temperature Sensor<br>0x0 : 100kHz   0x2 : 50kHz<br>0x1 : 200kHz   0x3 : Chopper Off        |
| 9:8            |          | 0x0                       | ExtTemp3ChpMode   | PGA Chopper Mode External Temperature Sensor T3<br>0x0 : 100kHz   0x2 : 50kHz<br>0x1 : 200kHz   0x3 : Chopper Off |
| 7:6            |          | 0x0                       | ExtTemp2ChpMode   | PGA Chopper Mode External Temperature Sensor T2<br>0x0 : 100kHz   0x2 : 50kHz<br>0x1 : 200kHz   0x3 : Chopper Off |
| 5:4            |          | 0x0                       | ExtTemp1ChpMode   | PGA Chopper Mode External Temperature Sensor T1<br>0x0 : 100kHz   0x2 : 50kHz<br>0x1 : 200kHz   0x3 : Chopper Off |
| 3:2            |          | 0x0                       | BM2ChpMode        | PGA Chopper Mode Bridge Sensor 2<br>0x0 : 100kHz   0x2 : 50kHz<br>0x1 : 200kHz   0x3 : Chopper Off                |
| 1:0            |          | 0x0                       | BM1ChpMode        | PGA Chopper Mode Bridge Sensor 1<br>0x0 : 100kHz   0x2 : 50kHz<br>0x1 : 200kHz   0x3 : Chopper Off                |

## 12.14 Output Clipping, Diagnostic Range Assignment and Watchdog

### 12.14.1 0x31 – DiagClipOutCfg.SysDiagCfg

| Address : 0x31 |          | Register Name : DiagClipOutCfg.SysDiagCfg |                    | Default: 0x00000000   |
|----------------|----------|---|--------------------|---|
| Bits           | Access   | Default                                   | Field Name         | Description   |
| 31:28          | Reserved | 0x0                                       |                    | Reserved  |
| 27:24          |          | 0x0                                       | WatchdogTimeout    | Watchdog Timeout<br>0x0 : 8ms    0x4 : 40ms    0x8 : 100ms    0xC : 1s<br>0x1 : 10ms    0x5 : 50ms    0x9 : 150ms    0xD : 2s<br>0x2 : 20ms    0x6 : 60ms    0xA : 200ms    0xE : 4s<br>0x3 : 30ms    0x7 : 80ms    0xB : 500ms    0xF : 8s   |
| 23:16          |          | 0x0                                       | WatchdogDisableKey | Watchdog Disable Key<br>0xA5 : Watchdog disabled<br>All other codes enable watchdog   |
| 15:2           | Reserved | 0x0                                       |                    | Reserved  |
| 1              |          | 0x0                                       | ClipOutEn          | Two-Sided Clipping to Upper and Lower Diagnostic Limit<br>0x0 : Disabled<br>0x1 : Enabled<br><b>Note:</b> Enabling this feature requires enabling ClipOutEn.<br><b>Note:</b> DiagOutEn sets the AOUI to either 0% (LDR) or 100% (UDR)<br><br>Failure signalization of saturation requires enabling of any additional AFE or sensor diagnosis functions. |
| 0              |          | 0x0                                       | DiagOutEn          | Output Signalization of Diagnostic State at AOUI<br>0x0 : Disabled<br>0x1 : Enabled<br><b>Note:</b> Clipping limits are defined in DiagClipOutCfg.ClipOutLvl register.  |

### 12.14.2 0x32 – DiagClipOutCfg.DiagOutLvl[0]

| Address : 0x32 |        | Register Name : DiagClipOutCfg.DiagOutLvl[0] |               | Default: 0x00007FFE   |
|----------------|--------|--|---------------|---|
| Bits           | Access | Default                                      | Field Name    | Description   |
| 31:0           |        | 0x7FFE                                       | DiagOutLvl[0] | Select register for UDR / LDR assignment of diagnostic checks |

### 12.14.3 0x33 – DiagClipOutCfg.DiagOutLvl[1]

| Address : 0x33 |        | Register Name : DiagClipOutCfg.DiagOutLvl[1] |               | Default: 0x00000000   |
|----------------|--------|--|---------------|---|
| Bits           | Access | Default                                      | Field Name    | Description   |
| 31:0           |        | 0x0  | DiagOutLvl[1] | Select register for UDR / LDR assignment of diagnostic checks |

### 12.14.4 0x34 – DiagClipOutCfg.DiagOutLvl[2]

| Address : 0x34 |        | Register Name : DiagClipOutCfg.DiagOutLvl[2] |               | Default: 0x0000003F |
|----------------|--------|--|---------------|---------------------|
| Bits           | Access | Default                                      | Field Name    | Description         |
| 31:0           |        | 0x3F   | DiagOutLvl[2] |                     |

### 12.14.5 0x35 – DiagClipOutCfg.ClipOutLvl

| Address : 0x35 |        | Register Name : DiagClipOutCfg.ClipOutLvl |             | Default: 0xF3330CCC                             |
|----------------|--------|---|-------------|---|
| Bits           | Access | Default                                   | Field Name  | Description                                     |
| 31:16          |        | 0xF333                                    | ClipOutHigh | Upper Clipping Limit<br>0xF333 : 95% Full Scale |
| 15:0           |        | 0xCCC                                     | ClipOutLow  | Lower Clipping Limit<br>0x0CCC : 5% Full Scale  |

## 12.15 SSC Coefficients

### 12.15.1 0x36 – Bs1Coeff.SOffset

| Address : 0x36 |          | Register Name : Bs1Coeff.SOffset |            | Default: 0x00000000                |
|----------------|----------|----------------------------------|------------|------------------------------------|
| Bits           | Access   | Default                          | Field Name | Description                        |
| 31:24          | Reserved | 0x0                              |            | Reserved                           |
| 23:0           |          | 0x0                              | SOffset    | Sensor offset term <i>Offset_S</i> |

### 12.15.2 0x37 – Bs1Coeff.SGain

| Address : 0x37 |          | Register Name : Bs1Coeff.SGain |            | Default: 0x00200000            |
|----------------|----------|--------------------------------|------------|--------------------------------|
| Bits           | Access   | Default                        | Field Name | Description                    |
| 31:24          | Reserved | 0x0                            |            | Reserved                       |
| 23:0           |          | 0x200000                       | SGain      | Sensor gain term <i>Gain_S</i> |

### 12.15.3 0x38 – Bs1Coeff.SSot

| Address : 0x38 |          | Register Name : Bs1Coeff.SSot |            | Default: 0x00000000  |
|----------------|----------|-------------------------------|------------|--|
| Bits           | Access   | Default                       | Field Name | Description  |
| 31:24          | Reserved | 0x0                           |            | Reserved   |
| 23:0           |          | 0x0                           | SSot       | Second-order term for sensor non-linearity <i>SOT_sens</i> |

### 12.15.4 0x39 – Bs1Coeff.SShift

| Address : 0x39 |          | Register Name : Bs1Coeff.SShift |            | Default: 0x00000000                     |
|----------------|----------|---------------------------------|------------|---|
| Bits           | Access   | Default                         | Field Name | Description                             |
| 31:24          | Reserved | 0x0                             |            | Reserved                                |
| 23:0           |          | 0x0                             | SShift     | Post-calibration term <i>SENS_shift</i> |

### 12.15.5 0x3A – Bs1Coeff.STco

| Address : 0x3A |          | Register Name : Bs1Coeff.STco |            | Default: 0x00000000                            |
|----------------|----------|-------------------------------|------------|--|
| Bits           | Access   | Default                       | Field Name | Description                                    |
| 31:24          | Reserved | 0x0                           |            | Reserved                                       |
| 23:0           |          | 0x0                           | STco       | Temperature coefficient offset term <i>Tco</i> |

### 12.15.6 0x3B – Bs1Coeff.SSotTco

| Address : 0x3B |          | Register Name : Bs1Coeff.SSotTco |            | Default: 0x00000000                                   |
|----------------|----------|----------------------------------|------------|---|
| Bits           | Access   | Default                          | Field Name | Description   |
| 31:24          | Reserved | 0x0                              |            | Reserved  |
| 23:0           |          | 0x0                              | SSotTco    | Second-order term for Tco nonlinearity <i>SOT_tco</i> |

### 12.15.7 0x3C – Bs1Coeff.STcg

| Address : 0x3C |          | Register Name : Bs1Coeff.STcg |            | Default: 0x00000000                          |
|----------------|----------|-------------------------------|------------|--|
| Bits           | Access   | Default                       | Field Name | Description                                  |
| 31:24          | Reserved | 0x0                           |            | Reserved                                     |
| 23:0           |          | 0x0                           | STcg       | Temperature coefficient gain term <i>Tcg</i> |

### 12.15.8 0x3D – Bs1Coeff.SSotTcg

| Address : 0x3D |          | Register Name : Bs1Coeff.SSotTcg |            | Default: 0x00000000                                    |
|----------------|----------|----------------------------------|------------|--|
| Bits           | Access   | Default                          | Field Name | Description  |
| 31:24          | Reserved | 0x0                              |            | Reserved   |
| 23:0           |          | 0x0                              | SSotTcg    | Second-order term for Tcg non-linearity <i>SOT_tcg</i> |

**12.15.9 0x3E – Bs1Coeff.OutScaleGain**

| <b>Address : 0x3E</b> |          | <b>Register Name : Bs1Coeff.OutScaleGain</b> |              | Default: 0x00100000          |
|-----------------------|----------|--|--------------|------------------------------|
| Bits                  | Access   | Default                                      | Field Name   | Description                  |
| 31:24                 | Reserved | 0x0  |              | Reserved                     |
| 23:0                  |          | 0x100000                                     | OutScaleGain | Post SSC Output Scaling Gain |

**12.15.10 0x3F – Bs1Coeff.OutScaleOfst**

| <b>Address : 0x3F</b> |          | <b>Register Name : Bs1Coeff.OutScaleOfst</b> |              | Default: 0x00000000            |
|-----------------------|----------|--|--------------|--------------------------------|
| Bits                  | Access   | Default                                      | Field Name   | Description                    |
| 31:24                 | Reserved | 0x0  |              | Reserved                       |
| 23:0                  |          | 0x0  | OutScaleOfst | Post SSC Output Scaling Offset |

**12.15.11 0x40 – Bs2Coeff.SOffset**

| <b>Address : 0x40</b> |          | <b>Register Name : Bs2Coeff.SOffset</b> |            | Default: 0x00000000                |
|-----------------------|----------|---|------------|------------------------------------|
| Bits                  | Access   | Default                                 | Field Name | Description                        |
| 31:24                 | Reserved | 0x0                                     |            | Reserved                           |
| 23:0                  |          | 0x0                                     | SOffset    | Sensor offset term <i>Offset_S</i> |

**12.15.12 0x41 – Bs2Coeff.SGain**

| <b>Address : 0x41</b> |          | <b>Register Name : Bs2Coeff.SGain</b> |            | Default: 0x00200000            |
|-----------------------|----------|---------------------------------------|------------|--------------------------------|
| Bits                  | Access   | Default                               | Field Name | Description                    |
| 31:24                 | Reserved | 0x0                                   |            | Reserved                       |
| 23:0                  |          | 0x200000                              | SGain      | Sensor gain term <i>Gain_S</i> |

**12.15.13 0x42 – Bs2Coeff.SSot**

| <b>Address : 0x42</b> |          | <b>Register Name : Bs2Coeff.SSot</b> |            | Default: 0x00000000  |
|-----------------------|----------|--------------------------------------|------------|--|
| Bits                  | Access   | Default                              | Field Name | Description  |
| 31:24                 | Reserved | 0x0                                  |            | Reserved   |
| 23:0                  |          | 0x0                                  | SSot       | Second-order term for sensor non-linearity <i>SOT_sens</i> |

**12.15.14 0x43 – Bs2Coeff.SShift**

| <b>Address : 0x43</b> |          | <b>Register Name : Bs2Coeff.SShift</b> |            | Default: 0x00000000                     |
|-----------------------|----------|--|------------|---|
| Bits                  | Access   | Default                                | Field Name | Description                             |
| 31:24                 | Reserved | 0x0                                    |            | Reserved                                |
| 23:0                  |          | 0x0                                    | SShift     | Post-calibration term <i>SENS_shift</i> |

**12.15.15 0x44 – Bs2Coeff.STco**

| <b>Address : 0x44</b> |          | <b>Register Name : Bs2Coeff.STco</b> |            | Default: 0x00000000                            |
|-----------------------|----------|--------------------------------------|------------|--|
| Bits                  | Access   | Default                              | Field Name | Description                                    |
| 31:24                 | Reserved | 0x0                                  |            | Reserved                                       |
| 23:0                  |          | 0x0                                  | STco       | Temperature coefficient offset term <i>Tco</i> |

**12.15.16 0x45 – Bs2Coeff.SSotTco**

| <b>Address : 0x45</b> |          | <b>Register Name : Bs2Coeff.SSotTco</b> |            | Default: 0x00000000                                   |
|-----------------------|----------|---|------------|---|
| Bits                  | Access   | Default                                 | Field Name | Description   |
| 31:24                 | Reserved | 0x0                                     |            | Reserved  |
| 23:0                  |          | 0x0                                     | SSotTco    | Second-order term for Tco nonlinearity <i>SOT_tco</i> |

## 12.15.17 0x46 – Bs2Coeff.STcg

| Address : 0x46 |          | Register Name : Bs2Coeff.STcg |            | Default: 0x00000000                          |
|----------------|----------|-------------------------------|------------|--|
| Bits           | Access   | Default                       | Field Name | Description                                  |
| 31:24          | Reserved | 0x0                           |            | Reserved                                     |
| 23:0           |          | 0x0                           | STcg       | Temperature coefficient gain term <i>Tcg</i> |

## 12.15.18 0x47 – Bs2Coeff.SSotTcg

| Address : 0x47 |          | Register Name : Bs2Coeff.SSotTcg |            | Default: 0x00000000   |
|----------------|----------|----------------------------------|------------|---|
| Bits           | Access   | Default                          | Field Name | Description   |
| 31:24          | Reserved | 0x0                              |            | Reserved  |
| 23:0           |          | 0x0                              | SSotTcg    | Second-order term for <i>Tcg</i> non-linearity <i>SOT_tcg</i> |

## 12.15.19 0x48 – Bs2Coeff.OutScaleGain

| Address : 0x48 |          | Register Name : Bs2Coeff.OutScaleGain |              | Default: 0x00100000          |
|----------------|----------|---------------------------------------|--------------|------------------------------|
| Bits           | Access   | Default                               | Field Name   | Description                  |
| 31:24          | Reserved | 0x0                                   |              | Reserved                     |
| 23:0           |          | 0x100000                              | OutScaleGain | Post SSC Output Scaling Gain |

## 12.15.20 0x49 – Bs2Coeff.OutScaleOfst

| Address : 0x49 |          | Register Name : Bs2Coeff.OutScaleOfst |              | Default: 0x00000000            |
|----------------|----------|---------------------------------------|--------------|--------------------------------|
| Bits           | Access   | Default                               | Field Name   | Description                    |
| 31:24          | Reserved | 0x0                                   |              | Reserved                       |
| 23:0           |          | 0x0                                   | OutScaleOfst | Post SSC Output Scaling Offset |

## 12.15.21 0x4A – Tch1Coeff.TOffset

| Address : 0x4A |          | Register Name : Tch1Coeff.TOffset |            | Default: 0x00000000                                |
|----------------|----------|-----------------------------------|------------|--|
| Bits           | Access   | Default                           | Field Name | Description  |
| 31:24          | Reserved | 0x0                               |            | Reserved   |
| 23:0           |          | 0x0                               | TOffset    | Offset coefficient for temperature <i>Offset_T</i> |

## 12.15.22 0x4B – Tch1Coeff.TGain

| Address : 0x4B |          | Register Name : Tch1Coeff.TGain |            | Default: 0x00200000                            |
|----------------|----------|---------------------------------|------------|--|
| Bits           | Access   | Default                         | Field Name | Description                                    |
| 31:24          | Reserved | 0x0                             |            | Reserved                                       |
| 23:0           |          | 0x200000                        | TGain      | Gain coefficient for temperature <i>Gain_T</i> |

## 12.15.23 0x4C – Tch1Coeff.TSot

| Address : 0x4C |          | Register Name : Tch1Coeff.TSot |            | Default: 0x00000000                                   |
|----------------|----------|--------------------------------|------------|---|
| Bits           | Access   | Default                        | Field Name | Description   |
| 31:24          | Reserved | 0x0                            |            | Reserved  |
| 23:0           |          | 0x0                            | TSot       | Second-order term for temperature source <i>SOT_T</i> |

## 12.15.24 0x4D – Tch1Coeff.TShift

| Address : 0x4D |          | Register Name : Tch1Coeff.TShift |            | Default: 0x00000000   |
|----------------|----------|----------------------------------|------------|---|
| Bits           | Access   | Default                          | Field Name | Description   |
| 31:24          | Reserved | 0x0                              |            | Reserved  |
| 23:0           |          | 0x0                              | TShift     | Shift for post-calibration/post-assembly offset compensation <i>T_Shift</i> |



12.15.25 0x4E – Tch2Coeff.TOffset

| Address : 0x4E |          | Register Name : Tch2Coeff.TOffset |            | Default: 0x00000000                                |
|----------------|----------|-----------------------------------|------------|--|
| Bits           | Access   | Default                           | Field Name | Description  |
| 31:24          | Reserved | 0x0                               |            | Reserved   |
| 23:0           |          | 0x0                               | TOffset    | Offset coefficient for temperature <i>Offset_T</i> |

12.15.26 0x4F – Tch2Coeff.TGain

| Address : 0x4F |          | Register Name : Tch2Coeff.TGain |            | Default: 0x00200000                            |
|----------------|----------|---------------------------------|------------|--|
| Bits           | Access   | Default                         | Field Name | Description                                    |
| 31:24          | Reserved | 0x0                             |            | Reserved                                       |
| 23:0           |          | 0x200000                        | TGain      | Gain coefficient for temperature <i>Gain_T</i> |

12.15.27 0x50 – Tch2Coeff.TSot

| Address : 0x50 |          | Register Name : Tch2Coeff.TSot |            | Default: 0x00000000                                   |
|----------------|----------|--------------------------------|------------|---|
| Bits           | Access   | Default                        | Field Name | Description   |
| 31:24          | Reserved | 0x0                            |            | Reserved  |
| 23:0           |          | 0x0                            | TSot       | Second-order term for temperature source <i>SOT_T</i> |

12.15.28 0x51 – Tch2Coeff.TShift

| Address : 0x51 |          | Register Name : Tch2Coeff.TShift |            | Default: 0x00000000   |
|----------------|----------|----------------------------------|------------|---|
| Bits           | Access   | Default                          | Field Name | Description   |
| 31:24          | Reserved | 0x0                              |            | Reserved  |
| 23:0           |          | 0x0                              | TShift     | Shift for post-calibration/post-assembly offset compensation <i>T_Shift</i> |

12.15.29 0x52 – Tch3Coeff.TOffset

| Address : 0x52 |          | Register Name : Tch3Coeff.TOffset |            | Default: 0x00000000                                |
|----------------|----------|-----------------------------------|------------|--|
| Bits           | Access   | Default                           | Field Name | Description  |
| 31:24          | Reserved | 0x0                               |            | Reserved   |
| 23:0           |          | 0x0                               | TOffset    | Offset coefficient for temperature <i>Offset_T</i> |

12.15.30 0x53 – Tch3Coeff.TGain

| Address : 0x53 |          | Register Name : Tch3Coeff.TGain |            | Default: 0x00200000                            |
|----------------|----------|---------------------------------|------------|--|
| Bits           | Access   | Default                         | Field Name | Description                                    |
| 31:24          | Reserved | 0x0                             |            | Reserved                                       |
| 23:0           |          | 0x200000                        | TGain      | Gain coefficient for temperature <i>Gain_T</i> |

12.15.31 0x54 – Tch3Coeff.TSot

| Address : 0x54 |          | Register Name : Tch3Coeff.TSot |            | Default: 0x00000000                                   |
|----------------|----------|--------------------------------|------------|---|
| Bits           | Access   | Default                        | Field Name | Description   |
| 31:24          | Reserved | 0x0                            |            | Reserved  |
| 23:0           |          | 0x0                            | TSot       | Second-order term for temperature source <i>SOT_T</i> |

12.15.32 0x55 – Tch3Coeff.TShift

| Address : 0x55 |          | Register Name : Tch3Coeff.TShift |            | Default: 0x00000000   |
|----------------|----------|----------------------------------|------------|---|
| Bits           | Access   | Default                          | Field Name | Description   |
| 31:24          | Reserved | 0x0                              |            | Reserved  |
| 23:0           |          | 0x0                              | TShift     | Shift for post-calibration/post-assembly offset compensation <i>T_Shift</i> |

## 12.16 CCP CRC

### 12.16.1 0x7F – CrcCcp0

| Address : 0x7F |        | Register Name : CrcCcp0 |            | Default: 0xEFD78925 |
|----------------|--------|-------------------------|------------|---------------------|
| Bits           | Access | Default                 | Field Name | Description         |
| 31:0           |        | 0xEFD78925              | CrcCcp0    |                     |

## 12.17 IO-Link – SI Scaling

### 12.17.1 0xA0 – SiScaling.Coeff[0].Offset

| Address : 0xA0 |        | Register Name : SiScaling.Coeff[0].Offset |            | Default: 0xFFFF8300        |
|----------------|--------|---|------------|----------------------------|
| Bits           | Access | Default                                   | Field Name | Description                |
| 31:0           |        | 0xFFFF8300                                | Offset     | SI Scaling Offset for MDC1 |

### 12.17.2 0xA1 – SiScaling.Coeff[0].Gain

| Address : 0xA1 |        | Register Name : SiScaling.Coeff[0].Gain |            | Default: 0x0000FA0       |
|----------------|--------|---|------------|--------------------------|
| Bits           | Access | Default                                 | Field Name | Description              |
| 31:0           |        | 0xFA0                                   | Gain       | SI Scaling Gain for MDC1 |

### 12.17.3 0xA2 – SiScaling.Coeff[1].Offset

| Address : 0xA2 |        | Register Name : SiScaling.Coeff[1].Offset |            | Default: 0xFFFF8000                             |
|----------------|--------|---|------------|---|
| Bits           | Access | Default                                   | Field Name | Description                                     |
| 31:0           |        | 0xFFFF8000                                | Offset     | SI Scaling Offset for MDC2 (n.a. for SSP 4.1.1) |

### 12.17.4 0xA3 – SiScaling.Coeff[1].Gain

| Address : 0xA3 |        | Register Name : SiScaling.Coeff[1].Gain |            | Default: 0x00001000                           |
|----------------|--------|---|------------|---|
| Bits           | Access | Default                                 | Field Name | Description                                   |
| 31:0           |        | 0x1000                                  | Gain       | SI Scaling Gain for MDC2 (n.a. for SSP 4.1.1) |

### 12.17.5 0xA4 – SiScaling.Coeff[2].Offset

| Address : 0xA4 |        | Register Name : SiScaling.Coeff[2].Offset |            | Default: 0xFFFF8000                             |
|----------------|--------|---|------------|---|
| Bits           | Access | Default                                   | Field Name | Description                                     |
| 31:0           |        | 0xFFFF8000                                | Offset     | SI Scaling Offset for MDC3 (n.a. for SSP 4.1.1) |

### 12.17.6 0xA5 – SiScaling.Coeff[2].Gain

| Address : 0xA5 |        | Register Name : SiScaling.Coeff[2].Gain |            | Default: 0x00001000                           |
|----------------|--------|---|------------|---|
| Bits           | Access | Default                                 | Field Name | Description                                   |
| 31:0           |        | 0x1000                                  | Gain       | SI Scaling Gain for MDC3 (n.a. for SSP 4.1.1) |

### 12.17.7 0xA6 – SiScaling.Coeff[3].Offset

| Address : 0xA6 |        | Register Name : SiScaling.Coeff[3].Offset |            | Default: 0xFFFF8000                             |
|----------------|--------|---|------------|---|
| Bits           | Access | Default                                   | Field Name | Description                                     |
| 31:0           |        | 0xFFFF8000                                | Offset     | SI Scaling Offset for MDC4 (n.a. for SSP 4.1.1) |

### 12.17.8 0xA7 – SiScaling.Coeff[3].Gain

| Address : 0xA7 |        | Register Name : SiScaling.Coeff[3].Gain |            | Default: 0x00001000                           |
|----------------|--------|---|------------|---|
| Bits           | Access | Default                                 | Field Name | Description                                   |
| 31:0           |        | 0x1000                                  | Gain       | SI Scaling Gain for MDC4 (n.a. for SSP 4.1.1) |

**12.17.9 0xA8 – SiScaling.OffsetScaler**

| Address : 0xA8 |        | Register Name : SiScaling.OffsetScaler |            | Default: 0x01010101                                    |
|----------------|--------|--|------------|--|
| Bits           | Access | Default                                | Field Name | Description  |
| 31:24          |        | 0x1                                    | Ch4        | SI Scaling Offset Scaler for MDC4 (n.a. for SSP 4.1.1) |
| 23:16          |        | 0x1                                    | Ch3        | SI Scaling Offset Scaler for MDC3 (n.a. for SSP 4.1.1) |
| 15:8           |        | 0x1                                    | Ch2        | SI Scaling Offset Scaler for MDC2 (n.a. for SSP 4.1.1) |
| 7:0            |        | 0x1                                    | Ch1        | SI Scaling Offset Scaler for MDC1 (n.a. for SSP 4.1.1) |

**12.18 IO-Link – Measurement Data Channel (MDC) Description****12.18.1 0xA9 – MdcDescr[0].LowerValue**

| Address : 0xA9 |        | Register Name : MdcDescr[0].LowerValue |            | Default: 0xFFFF8300   |
|----------------|--------|--|------------|---|
| Bits           | Access | Default                                | Field Name | Description   |
| 31:0           |        | 0xFFFF8300                             | LowerValue | Lower value of measurement range for MDC1 - transmitted in ISDU 0x4080 Subindex 0x1 |

**12.18.2 0xAA – MdcDescr[0].UpperValue**

| Address : 0xAA |        | Register Name : MdcDescr[0].UpperValue |            | Default: 0x00007D00   |
|----------------|--------|--|------------|---|
| Bits           | Access | Default                                | Field Name | Description   |
| 31:0           |        | 0x7D00                                 | UpperValue | Upper value of measurement range for MDC1 - transmitted in ISDU 0x4080 Subindex 0x2 |

**12.18.3 0xAB – MdcDescr[0].Reg1**

| Address : 0xAB |        | Register Name : MdcDescr[0].Reg1 |            | Default: 0x0003046A   |
|----------------|--------|----------------------------------|------------|---|
| Bits           | Access | Default                          | Field Name | Description   |
| 31:24          |        | 0x0                              | Unused     | Unused  |
| 23:16          |        | 0x3                              | Scale      | Range shifting (10scale) for MDC1 - transmitted in ISDU 0x4080 Subindex 0x4 |
| 15:0           |        | 0x46A                            | UnitCode   | Unit Code (SI unit) for MDC1 - transmitted in ISDU 0x4080 Subindex 0x3      |

**12.18.4 0xAC – MdcDescr[1].LowerValue**

| Address : 0xAC |        | Register Name : MdcDescr[1].LowerValue |            | Default: 0x00000000  |
|----------------|--------|--|------------|--|
| Bits           | Access | Default                                | Field Name | Description  |
| 31:0           |        | 0x0                                    | LowerValue | Lower value of measurement range for MDC2 (n.a. for SSP 4.1.1) |

**12.18.5 0xAD – MdcDescr[1].UpperValue**

| Address : 0xAD |        | Register Name : MdcDescr[1].UpperValue |            | Default: 0x00000000  |
|----------------|--------|--|------------|--|
| Bits           | Access | Default                                | Field Name | Description  |
| 31:0           |        | 0x0                                    | UpperValue | Upper value of measurement range for MDC2 (n.a. for SSP 4.1.1) |

**12.18.6 0xAE – MdcDescr[1].Reg1**

| Address : 0xAE |        | Register Name : MdcDescr[1].Reg1 |            | Default: 0x00000000                                    |
|----------------|--------|----------------------------------|------------|--|
| Bits           | Access | Default                          | Field Name | Description  |
| 31:24          |        | 0x0                              | Unused     | Unused (n.a. for SSP 4.1.1)                            |
| 23:16          |        | 0x0                              | Scale      | Range shifting (10scale) for MDC2 (n.a. for SSP 4.1.1) |
| 15:0           |        | 0x0                              | UnitCode   | Unit Code (SI unit) for MDC2 (n.a. for SSP 4.1.1)      |

**12.18.7 0xAF – MdcDescr[2].LowerValue**

| Address : 0xAF |        | Register Name : MdcDescr[2].LowerValue |            | Default: 0x00000000  |
|----------------|--------|--|------------|--|
| Bits           | Access | Default                                | Field Name | Description  |
| 31:0           |        | 0x0                                    | LowerValue | Lower value of measurement range for MDC3 (n.a. for SSP 4.1.1) |

**12.18.8 0xB0 – MdcDescr[2].UpperValue**

| Address : 0xB0 |        | Register Name : MdcDescr[2].UpperValue |            | Default: 0x00000000  |
|----------------|--------|--|------------|--|
| Bits           | Access | Default                                | Field Name | Description  |
| 31:0           |        | 0x0                                    | UpperValue | Upper value of measurement range for MDC3 (n.a. for SSP 4.1.1) |

**12.18.9 0xB1 – MdcDescr[2].Reg1**

| Address : 0xB1 |        | Register Name : MdcDescr[2].Reg1 |            | Default: 0x00000000                                    |
|----------------|--------|----------------------------------|------------|--|
| Bits           | Access | Default                          | Field Name | Description  |
| 31:24          |        | 0x0                              | Unused     | Unused (n.a. for SSP 4.1.1)                            |
| 23:16          |        | 0x0                              | Scale      | Range shifting (10scale) for MDC3 (n.a. for SSP 4.1.1) |
| 15:0           |        | 0x0                              | UnitCode   | Unit Code (SI unit) for MDC3 (n.a. for SSP 4.1.1)      |

**12.18.10 0xB2 – MdcDescr[3].LowerValue**

| Address : 0xB2 |        | Register Name : MdcDescr[3].LowerValue |            | Default: 0x00000000  |
|----------------|--------|--|------------|--|
| Bits           | Access | Default                                | Field Name | Description  |
| 31:0           |        | 0x0                                    | LowerValue | Lower value of measurement range for MDC4 (n.a. for SSP 4.1.1) |

**12.18.11 0xB3 – MdcDescr[3].UpperValue**

| Address : 0xB3 |        | Register Name : MdcDescr[3].UpperValue |            | Default: 0x00000000  |
|----------------|--------|--|------------|--|
| Bits           | Access | Default                                | Field Name | Description  |
| 31:0           |        | 0x0                                    | UpperValue | Upper value of measurement range for MDC4 (n.a. for SSP 4.1.1) |

**12.18.12 0xB4 – MdcDescr[3].Reg1**

| Address : 0xB4 |        | Register Name : MdcDescr[3].Reg1 |            | Default: 0x00000000                                    |
|----------------|--------|----------------------------------|------------|--|
| Bits           | Access | Default                          | Field Name | Description  |
| 31:24          |        | 0x0                              | Unused     | Unused (n.a. for SSP 4.1.1)                            |
| 23:16          |        | 0x0                              | Scale      | Range shifting (10scale) for MDC4 (n.a. for SSP 4.1.1) |
| 15:0           |        | 0x0                              | UnitCode   | Unit Code (SI unit) for MDC4 (n.a. for SSP 4.1.1)      |

**12.19 IO-Link – SSP Channel Mapping****12.19.1 0xB5 – SspChMap**

| Address : 0xB5 |          | Register Name : SspChMap |            | Default: 0x00006660  |
|----------------|----------|--------------------------|------------|--|
| Bits           | Access   | Default                  | Field Name | Description  |
| 31:16          | Reserved | 0x0                      |            | Reserved   |
| 15:12          |          | 0x6                      | Ch4        | Mapped DataChannel for MDC4 (n.a. for SSP 4.1.1)   |
| 11:8           |          | 0x6                      | Ch3        | Mapped Data Channel for MDC3 (n.a. for SSP 4.1.1)  |
| 7:4            |          | 0x6                      | Ch2        | Mapped Data Channel for MDC2 (n.a. for SSP 4.1.1)  |
| 3:0            |          | 0x0                      | Ch1        | Mapped Data Channel for MDC1<br>0x0 : Sensor Channel 1<br>0x1 : Sensor Channel 2<br>0x2 : Third Logic Channel 3<br>0x3 : Temperature Channel 1<br>0x4 : Temperature Channel 2<br>0x5 : Temperature Channel 3 |

**12.20 IO-Link – Vendor Text****12.20.1 0xB6 – VendorText[0]**

| Address : 0xB6 |        | Register Name : VendorText[0] |               | Default: 0x62206F54   |
|----------------|--------|-------------------------------|---------------|---|
| Bits           | Access | Default                       | Field Name    | Description   |
| 31:0           |        | 0x62206F54                    | VendorText[0] | Vendor Name - transmitted in ISDU 0x11 - characters 3, 2, 1, 0<br>Bits 31:24 : character 3<br>Bits 23:16 : character 2<br>Bits 15:8 : character 1<br>Bits 7:0 : character 0 |

**12.20.2 0xB7 – VendorText[1]**

| Address : 0xB7 |        | Register Name : VendorText[1] |               | Default: 0x69662065  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x69662065                    | VendorText[1] | Vendor Name - transmitted in ISDU 0x11 - characters 7, 6, 5, 4 |

**12.20.3 0xB8 – VendorText[2]**

| Address : 0xB8 |        | Register Name : VendorText[2] |               | Default: 0x64656C6C  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x64656C6C                    | VendorText[2] | Vendor Name - transmitted in ISDU 0x11 - characters 11, 10, 9, 8 |

**12.20.4 0xB9 – VendorText[3]**

| Address : 0xB9 |        | Register Name : VendorText[3] |               | Default: 0x20796220  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x20796220                    | VendorText[3] | Vendor Name - transmitted in ISDU 0x11 - characters 15, 14, 13, 12 |

**12.20.5 0xBA – VendorText[4]**

| Address : 0xBA |        | Register Name : VendorText[4] |               | Default: 0x656E6552  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x656E6552                    | VendorText[4] | Vendor Name - transmitted in ISDU 0x11 - characters 19, 18, 17, 16 |

**12.20.6 0xBB – VendorText[5]**

| Address : 0xBB |        | Register Name : VendorText[5] |               | Default: 0x20736173  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x20736173                    | VendorText[5] | Vendor Name - transmitted in ISDU 0x11 - characters 23, 22, 21, 20 |

**12.20.7 0xBC – VendorText[6]**

| Address : 0xBC |        | Register Name : VendorText[6] |               | Default: 0x74737563  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x74737563                    | VendorText[6] | Vendor Name - transmitted in ISDU 0x11 - characters 27, 26, 25, 24 |

**12.20.8 0xBD – VendorText[7]**

| Address : 0xBD |        | Register Name : VendorText[7] |               | Default: 0x72656D6F  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x72656D6F                    | VendorText[7] | Vendor Name - transmitted in ISDU 0x11 - characters 31, 30, 29, 28 |

**12.20.9 0xBE – VendorText[8]**

| Address : 0xBE |        | Register Name : VendorText[8] |               | Default: 0x00000000  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x0                           | VendorText[8] | Vendor Name - transmitted in ISDU 0x11 - characters 35, 34, 33, 32 |

**12.20.10 0xBF – VendorText[9]**

| Address : 0xBF |        | Register Name : VendorText[9] |               | Default: 0x00000000  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x0                           | VendorText[9] | Vendor Name - transmitted in ISDU 0x11 - characters 39, 38, 37, 36 |

**12.20.11 0xC0 – VendorText[10]**

| Address : 0xC0 |        | Register Name : VendorText[10] |                | Default: 0x00000000  |
|----------------|--------|--------------------------------|----------------|--|
| Bits           | Access | Default                        | Field Name     | Description  |
| 31:0           |        | 0x0                            | VendorText[10] | Vendor Name - transmitted in ISDU 0x11 - characters 43, 42, 41, 40 |

**12.20.12 0xC1 – VendorText[11]**

| Address : 0xC1 |        | Register Name : VendorText[11] |                | Default: 0x00000000  |
|----------------|--------|--------------------------------|----------------|--|
| Bits           | Access | Default                        | Field Name     | Description  |
| 31:0           |        | 0x0                            | VendorText[11] | Vendor Name - transmitted in ISDU 0x11 - characters 47, 46, 45, 44 |

**12.21 IO-Link – Product Text****12.21.1 0xC2 – ProductText[0]**

| Address : 0xC2 |        | Register Name : ProductText[0] |                | Default: 0x62206F54  |
|----------------|--------|--------------------------------|----------------|--|
| Bits           | Access | Default                        | Field Name     | Description  |
| 31:0           |        | 0x62206F54                     | ProductText[0] | Product Text - transmitted in ISDU 0x14 - characters 3, 2, 1, 0<br>Bits 31:24 : character 3<br>Bits 23:16 : character 2<br>Bits 15:8 : character 1<br>Bits 7:0 : character 0 |

**12.21.2 0xC3 – ProductText[1]**

| Address : 0xC3 |        | Register Name : ProductText[1] |                | Default: 0x69662065   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x69662065                     | ProductText[1] | Product Text - transmitted in ISDU 0x14 - characters 7, 6, 5, 4 |

**12.21.3 0xC4 – ProductText[2]**

| Address : 0xC4 |        | Register Name : ProductText[2] |                | Default: 0x64656C6C   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x64656C6C                     | ProductText[2] | Product Text - transmitted in ISDU 0x14 - characters 11, 10, 9, 8 |

**12.21.4 0xC5 – ProductText[3]**

| Address : 0xC5 |        | Register Name : ProductText[3] |                | Default: 0x20796220   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x20796220                     | ProductText[3] | Product Text - transmitted in ISDU 0x14 - characters 15, 14, 13, 12 |

**12.21.5 0xC6 – ProductText[4]**

| Address : 0xC6 |        | Register Name : ProductText[4] |                | Default: 0x656E6552   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x656E6552                     | ProductText[4] | Product Text - transmitted in ISDU 0x14 - characters 19, 18, 17, 16 |

**12.21.6 0xC7 – ProductText[5]**

| Address : 0xC7 |        | Register Name : ProductText[5] |                | Default: 0x20736173   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x20736173                     | ProductText[5] | Product Text - transmitted in ISDU 0x14 - characters 23, 22, 21, 20 |

**12.21.7 0xC8 – ProductText[6]**

| Address : 0xC8 |        | Register Name : ProductText[6] |                | Default: 0x74737563   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x74737563                     | ProductText[6] | Product Text - transmitted in ISDU 0x14 - characters 27, 26, 25, 24 |

**12.21.8 0xC9 – ProductText[7]**

| Address : 0xC9 |        | Register Name : ProductText[7] |                | Default: 0x72656D6F   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x72656D6F                     | ProductText[7] | Product Text - transmitted in ISDU 0x14 - characters 31, 30, 29, 28 |

**12.21.9 0xCA – ProductText[8]**

| Address : 0xCA |        | Register Name : ProductText[8] |                | Default: 0x00000000   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x0                            | ProductText[8] | Product Text - transmitted in ISDU 0x14 - characters 35, 34, 33, 32 |

**12.21.10 0xCB – ProductText[9]**

| Address : 0xCB |        | Register Name : ProductText[9] |                | Default: 0x00000000   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x0                            | ProductText[9] | Product Text - transmitted in ISDU 0x14 - characters 39, 38, 37, 36 |

**12.21.11 0xCC – ProductText[10]**

| Address : 0xCC |        | Register Name : ProductText[10] |                 | Default: 0x00000000   |
|----------------|--------|---------------------------------|-----------------|---|
| Bits           | Access | Default                         | Field Name      | Description   |
| 31:0           |        | 0x0                             | ProductText[10] | Product Text - transmitted in ISDU 0x14 - characters 43, 42, 41, 40 |

**12.21.12 0xCD – ProductText[11]**

| Address : 0xCD |        | Register Name : ProductText[11] |                 | Default: 0x00000000   |
|----------------|--------|---------------------------------|-----------------|---|
| Bits           | Access | Default                         | Field Name      | Description   |
| 31:0           |        | 0x0                             | ProductText[11] | Product Text - transmitted in ISDU 0x14 - characters 47, 46, 45, 44 |

**12.22 IO-Link – Serial Number****12.22.1 0xCE – SerialNumber[0]**

| Address : 0xCE |        | Register Name : SerialNumber[0] |                 | Default: 0x62206F54   |
|----------------|--------|---------------------------------|-----------------|---|
| Bits           | Access | Default                         | Field Name      | Description   |
| 31:0           |        | 0x62206F54                      | SerialNumber[0] | Serial Number - transmitted in ISDU 0x15 - characters 3, 2, 1, 0<br>Bits 31:24 : character 3<br>Bits 23:16 : character 2<br>Bits 15:8 : character 1<br>Bits 7:0 : character 0 |

**12.22.2 0xCF – SerialNumber[1]**

| Address : 0xCF |        | Register Name : SerialNumber[1] |                 | Default: 0x69662065  |
|----------------|--------|---------------------------------|-----------------|--|
| Bits           | Access | Default                         | Field Name      | Description  |
| 31:0           |        | 0x69662065                      | SerialNumber[1] | Serial Number - transmitted in ISDU 0x15 - characters 7, 6, 5, 4 |

**12.22.3 0xD0 – SerialNumber[2]**

| Address : 0xD0 |        | Register Name : SerialNumber[2] |                 | Default: 0x64656C6C  |
|----------------|--------|---------------------------------|-----------------|--|
| Bits           | Access | Default                         | Field Name      | Description  |
| 31:0           |        | 0x64656C6C                      | SerialNumber[2] | Serial Number - transmitted in ISDU 0x15 - characters 11, 10, 9, 8 |

12.22.4 0xD1 – SerialNumber[3]

| Address : 0xD1 |        | Register Name : SerialNumber[3] |                 | Default: 0x00000000  |
|----------------|--------|---------------------------------|-----------------|--|
| Bits           | Access | Default                         | Field Name      | Description  |
| 31:0           |        | 0x0                             | SerialNumber[3] | Serial Number - transmitted in ISDU 0x15 - characters 15, 14, 13, 12 |

12.23 IO-Link – Firmware Password

12.23.1 0xD2 – FwPassword[0]

If FW Password is other than empty String, the FW password function becomes effective.

| Address : 0xD2 |        | Register Name : FwPassword[0] |               | Default: 0x00000000   |
|----------------|--------|-------------------------------|---------------|---|
| Bits           | Access | Default                       | Field Name    | Description   |
| 31:0           |        | 0x0                           | FwPassword[0] | Firmware Password - transmitted in ISDU 0x43BD - characters 3, 2, 1, 0<br>Bits 31:24 : character 3<br>Bits 23:16 : character 2<br>Bits 15:8 : character 1<br>Bits 7:0 : character 0 |

12.23.2 0xD3 – FwPassword[1]

| Address : 0xD3 |        | Register Name : FwPassword[1] |               | Default: 0x00000000  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x0                           | FwPassword[1] | Firmware Password - transmitted in ISDU 0x43BD - characters 11, 10, 9, 8 |

12.23.3 0xD4 – FwPassword[2]

| Address : 0xD4 |        | Register Name : FwPassword[2] |               | Default: 0x00000000  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x0                           | FwPassword[2] | Firmware Password - transmitted in ISDU 0x43BD - characters 15, 14, 13, 12 |

12.23.4 0xD5 – FwPassword[3]

| Address : 0xD5 |        | Register Name : FwPassword[3] |               | Default: 0x00000000  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x0                           | FwPassword[3] | Firmware Password - transmitted in ISDU 0x43BD - characters 19, 18, 17, 16 |

12.24 IO-Link – Device IDs

12.24.1 0xD6 – Deviceld

Value 0x0 not allowed.

| Address : 0xD6 |        | Register Name : Deviceld |            | Default: 0x00000001  |
|----------------|--------|--------------------------|------------|--|
| Bits           | Access | Default                  | Field Name | Description  |
| 31:0           |        | 0x1                      | Deviceld   | Devide ID in active Firmware - transmitted in ISDU 0xA, 0xB, 0xC - LSB aligned |

12.24.2 0xD7 – BootloaderDeviceld

Value 0x0 not allowed.

| Address : 0xD7 |        | Register Name : BootloaderDeviceld |                    | Default: 0x00000002   |
|----------------|--------|------------------------------------|--------------------|---|
| Bits           | Access | Default                            | Field Name         | Description   |
| 31:0           |        | 0x2                                | BootloaderDeviceld | Device ID in Bootloader - transmitted in ISDU 0xA, 0xB, 0xC - LSB aligned |



## 12.25 IO-Link – Vendor ID

### 12.25.1 0xD8 – VendorId

| Address : 0xD8 |        | Register Name : VendorId |            | Default: 0x000018C  |
|----------------|--------|--------------------------|------------|---|
| Bits           | Access | Default                  | Field Name | Description   |
| 31:0           |        | 0x18C                    | VendorId   | Vendor ID - transmitted in ISDU 0x8 and 0x9 - LSB aligned |

## 12.26 IO-Link – Vendor Name

### 12.26.1 0xD9 – VendorName[0]

| Address : 0xD9 |        | Register Name : VendorName[0] |               | Default: 0x62206F54   |
|----------------|--------|-------------------------------|---------------|---|
| Bits           | Access | Default                       | Field Name    | Description   |
| 31:0           |        | 0x62206F54                    | VendorName[0] | Vendor Name - transmitted in ISDU 0x10 - characters 3, 2, 1, 0<br>Bits 31:24 : character 3<br>Bits 23:16 : character 2<br>Bits 15:8 : character 1<br>Bits 7:0 : character 0 |

### 12.26.2 0xDA – VendorName[1]

| Address : 0xDA |        | Register Name : VendorName[1] |               | Default: 0x69662065  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x69662065                    | VendorName[1] | Vendor Name - transmitted in ISDU 0x10 - characters 7, 6, 5, 4 |

### 12.26.3 0xDB – VendorName[2]

| Address : 0xDB |        | Register Name : VendorName[2] |               | Default: 0x64656C6C  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x64656C6C                    | VendorName[2] | Vendor Name - transmitted in ISDU 0x10 - characters 11, 10, 9, 8 |

### 12.26.4 0xDC – VendorName[3]

| Address : 0xDC |        | Register Name : VendorName[3] |               | Default: 0x20796220  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x20796220                    | VendorName[3] | Vendor Name - transmitted in ISDU 0x10 - characters 15, 14, 13, 12 |

### 12.26.5 0xDD – VendorName[4]

| Address : 0xDD |        | Register Name : VendorName[4] |               | Default: 0x656E6552  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x656E6552                    | VendorName[4] | Vendor Name - transmitted in ISDU 0x10 - characters 19, 18, 17, 16 |

### 12.26.6 0xDE – VendorName[5]

| Address : 0xDE |        | Register Name : VendorName[5] |               | Default: 0x20736173  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x20736173                    | VendorName[5] | Vendor Name - transmitted in ISDU 0x10 - characters 23, 22, 21, 20 |

### 12.26.7 0xDF – VendorName[6]

| Address : 0xDF |        | Register Name : VendorName[6] |               | Default: 0x74737563  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x74737563                    | VendorName[6] | Vendor Name - transmitted in ISDU 0x10 - characters 27, 26, 25, 24 |

**12.26.8 0xE0 – VendorName[7]**

| Address : 0xE0 |        | Register Name : VendorName[7] |               | Default: 0x72656D6F  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x72656D6F                    | VendorName[7] | Vendor Name - transmitted in ISDU 0x10 - characters 31, 30, 29, 28 |

**12.26.9 0xE1 – VendorName[8]**

| Address : 0xE1 |        | Register Name : VendorName[8] |               | Default: 0x00000000  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x0                           | VendorName[8] | Vendor Name - transmitted in ISDU 0x10 - characters 35, 34, 33, 32 |

**12.26.10 0xE2 – VendorName[9]**

| Address : 0xE2 |        | Register Name : VendorName[9] |               | Default: 0x00000000  |
|----------------|--------|-------------------------------|---------------|--|
| Bits           | Access | Default                       | Field Name    | Description  |
| 31:0           |        | 0x0                           | VendorName[9] | Vendor Name - transmitted in ISDU 0x10 - characters 39, 38, 37, 36 |

**12.26.11 0xE3 – VendorName[10]**

| Address : 0xE3 |        | Register Name : VendorName[10] |                | Default: 0x00000000  |
|----------------|--------|--------------------------------|----------------|--|
| Bits           | Access | Default                        | Field Name     | Description  |
| 31:0           |        | 0x0                            | VendorName[10] | Vendor Name - transmitted in ISDU 0x10 - characters 43, 42, 41, 40 |

**12.26.12 0xE4 – VendorName[11]**

| Address : 0xE4 |        | Register Name : VendorName[11] |                | Default: 0x00000000  |
|----------------|--------|--------------------------------|----------------|--|
| Bits           | Access | Default                        | Field Name     | Description  |
| 31:0           |        | 0x0                            | VendorName[11] | Vendor Name - transmitted in ISDU 0x10 - characters 47, 46, 45, 44 |

**12.27 IO-Link – Hardware ID Key****12.27.1 0xE5 – HwldKey[0]**

| Address : 0xE5 |        | Register Name : HwldKey[0] |            | Default: 0x425F4F54  |
|----------------|--------|----------------------------|------------|--|
| Bits           | Access | Default                    | Field Name | Description  |
| 31:0           |        | 0x425F4F54                 | HwldKey[0] | Hardware ID Key - transmitted in ISDU 0x43BE - characters 3, 2, 1, 0<br>Bits 31:24 : character 3<br>Bits 23:1 : character 2<br>Bits 15:8 : character 1<br>Bits 7:0 : character 0 |

**12.27.2 0xE6 – HwldKey[1]**

| Address : 0xE6 |        | Register Name : HwldKey[1] |            | Default: 0x49465F45  |
|----------------|--------|----------------------------|------------|--|
| Bits           | Access | Default                    | Field Name | Description  |
| 31:0           |        | 0x49465F45                 | HwldKey[1] | Hardware ID Key - transmitted in ISDU 0x43BE - characters 7, 6, 5, 4 |

**12.27.3 0xE7 – HwldKey[2]**

| Address : 0xE7 |        | Register Name : HwldKey[2] |            | Default: 0x44454C4C  |
|----------------|--------|----------------------------|------------|--|
| Bits           | Access | Default                    | Field Name | Description  |
| 31:0           |        | 0x44454C4C                 | HwldKey[2] | Hardware ID Key - transmitted in ISDU 0x43BE - characters 11, 10, 9, 8 |

**12.27.4 0xE8 – HwldKey[3]**

| Address : 0xE8 |        | Register Name : HwldKey[3] |            | Default: 0x00000000  |
|----------------|--------|----------------------------|------------|--|
| Bits           | Access | Default                    | Field Name | Description  |
| 31:0           |        | 0x0                        | HwldKey[3] | Hardware ID Key - transmitted in ISDU 0x43BE - characters 15, 14, 13, 12 |

## 12.28 IO-Link – Hardware Revision

### 12.28.1 0xE9 – HardwareRevision[0]

| Address : 0xE9 |        | Register Name : HardwareRevision[0] |                     | Default: 0x62206F54   |
|----------------|--------|-------------------------------------|---------------------|---|
| Bits           | Access | Default                             | Field Name          | Description   |
| 31:0           |        | 0x62206F54                          | HardwareRevision[0] | Hardware Revision - transmitted in ISDU 0x16 - characters 3, 2, 1, 0<br>Bits 31:24 : character 3<br>Bits 23:16 : character 2<br>Bits 15:8 : character 1<br>Bits 7:0 : character 0 |

### 12.28.2 0xEA – HardwareRevision[1]

| Address : 0xEA |        | Register Name : HardwareRevision[1] |                     | Default: 0x69662065  |
|----------------|--------|-------------------------------------|---------------------|--|
| Bits           | Access | Default                             | Field Name          | Description  |
| 31:0           |        | 0x69662065                          | HardwareRevision[1] | Hardware Revision - transmitted in ISDU 0x16 - characters 7, 6, 5, 4 |

### 12.28.3 0xEB – HardwareRevision[2]

| Address : 0xEB |        | Register Name : HardwareRevision[2] |                     | Default: 0x64656C6C  |
|----------------|--------|-------------------------------------|---------------------|--|
| Bits           | Access | Default                             | Field Name          | Description  |
| 31:0           |        | 0x64656C6C                          | HardwareRevision[2] | Hardware Revision - transmitted in ISDU 0x16 - characters 11, 10, 9, 8 |

### 12.28.4 0xEC – HardwareRevision[3]

| Address : 0xEC |        | Register Name : HardwareRevision[3] |                     | Default: 0x00000000  |
|----------------|--------|-------------------------------------|---------------------|--|
| Bits           | Access | Default                             | Field Name          | Description  |
| 31:0           |        | 0x0                                 | HardwareRevision[3] | Hardware Revision - transmitted in ISDU 0x16 - characters 15, 14, 13, 12 |

## 12.29 IO-Link – Product Name

### 12.29.1 0xED – ProductName

| Address : 0xED |        | Register Name : ProductName[0] |                | Default: 0x62206F54  |
|----------------|--------|--------------------------------|----------------|--|
| Bits           | Access | Default                        | Field Name     | Description  |
| 31:0           |        | 0x62206F54                     | ProductName[0] | Product Name - transmitted in ISDU 0x12 - characters 3, 2, 1, 0<br>Bits 31:24 : character 3<br>Bits 23:16 : character 2<br>Bits 15:8 : character 1<br>Bits 7:0 : character 0 |

| Address : 0xEE |        | Register Name : ProductName[1] |                | Default: 0x69662065   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x69662065                     | ProductName[1] | Product Name - transmitted in ISDU 0x12 - characters 7, 6, 5, 4 |

| Address : 0xEF |        | Register Name : ProductName[2] |                | Default: 0x64656C6C   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x64656C6C                     | ProductName[2] | Product Name - transmitted in ISDU 0x12 - characters 11, 10, 9, 8 |

| Address : 0xF0 |        | Register Name : ProductName[3] |                | Default: 0x20796220   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x20796220                     | ProductName[3] | Product Name - transmitted in ISDU 0x12 - characters 15, 14, 13, 12 |

| Address : 0xF1 |        | Register Name : ProductName[4] |                | Default: 0x656E6552   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x656E6552                     | ProductName[4] | Product Name - transmitted in ISDU 0x12 - characters 19, 18, 17, 16 |

| Address : 0xF2 |        | Register Name : ProductName[5] |                | Default: 0x20736173   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x20736173                     | ProductName[5] | Product Name - transmitted in ISDU 0x12 - characters 23, 22, 21, 20 |

| Address : 0xF3 |        | Register Name : ProductName[6] |                | Default: 0x74737563   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x74737563                     | ProductName[6] | Product Name - transmitted in ISDU 0x12 - characters 27, 26, 25, 24 |

| Address : 0xF4 |        | Register Name : ProductName[7] |                | Default: 0x72656D6F   |
|----------------|--------|--------------------------------|----------------|---|
| Bits           | Access | Default                        | Field Name     | Description   |
| 31:0           |        | 0x72656D6F                     | ProductName[7] | Product Name - transmitted in ISDU 0x12 - characters 31, 30, 29, 28 |

## 12.30 IO-Link – Product ID

### 12.30.1 0xF5 – ProductId

| Address : 0xF5 |        | Register Name : ProductId[0] |              | Default: 0x62206F54  |
|----------------|--------|------------------------------|--------------|--|
| Bits           | Access | Default                      | Field Name   | Description  |
| 31:0           |        | 0x62206F54                   | ProductId[0] | Product ID - transmitted in ISDU 0x13 - characters 3, 2, 1, 0<br>Bits 31:24 : character 3<br>Bits 23:16 : character 2<br>Bits 15:8 : character 1<br>Bits 7:0 : character 0 |

| Address : 0xF6 |        | Register Name : ProductId[1] |              | Default: 0x69662065   |
|----------------|--------|------------------------------|--------------|---|
| Bits           | Access | Default                      | Field Name   | Description   |
| 31:0           |        | 0x69662065                   | ProductId[1] | Product ID - transmitted in ISDU 0x13 - characters 7, 6, 5, 4 |

| Address : 0xF7 |        | Register Name : ProductId[2] |              | Default: 0x64656C6C   |
|----------------|--------|------------------------------|--------------|---|
| Bits           | Access | Default                      | Field Name   | Description   |
| 31:0           |        | 0x64656C6C                   | ProductId[2] | Product ID - transmitted in ISDU 0x13 - characters 11, 10, 9, 8 |

| Address : 0xF8 |        | Register Name : ProductId[3] |              | Default: 0x00000000   |
|----------------|--------|------------------------------|--------------|---|
| Bits           | Access | Default                      | Field Name   | Description   |
| 31:0           |        | 0x0                          | ProductId[3] | Product ID - transmitted in ISDU 0x13 - characters 15, 14, 13, 12 |

| Address : 0xF9 |        | Register Name : ProductId[4] |              | Default: 0x00000000   |
|----------------|--------|------------------------------|--------------|---|
| Bits           | Access | Default                      | Field Name   | Description   |
| 31:0           |        | 0x0                          | ProductId[4] | Product ID - transmitted in ISDU 0x13 - characters 19, 18, 17, 16 |

| Address : 0xFA |        | Register Name : ProductId[5] |              | Default: 0x00000000   |
|----------------|--------|------------------------------|--------------|---|
| Bits           | Access | Default                      | Field Name   | Description   |
| 31:0           |        | 0x0                          | ProductId[5] | Product ID - transmitted in ISDU 0x13 - characters 23, 22, 21, 20 |

| Address : 0xFB |        | Register Name : ProductId[6] |              | Default: 0x00000000   |
|----------------|--------|------------------------------|--------------|---|
| Bits           | Access | Default                      | Field Name   | Description   |
| 31:0           |        | 0x0                          | ProductId[6] | Product ID - transmitted in ISDU 0x13 - characters 27, 26, 25, 24 |

| Address : 0xFC |        | Register Name : ProductId[7] |              | Default: 0x00000000   |
|----------------|--------|------------------------------|--------------|---|
| Bits           | Access | Default                      | Field Name   | Description   |
| 31:0           |        | 0x0                          | ProductId[7] | Product ID - transmitted in ISDU 0x13 - characters 31, 30, 29, 28 |

## 12.31 CCP Password, Version and CRC

### 12.31.1 0xFD – CcpPassword

If CCP Password is different from 0xFFFFFFFF, CCP Password protection becomes effective.

| Address : 0xFD |        | Register Name : CcpPassword |             | Default: 0xFFFFFFFF  |
|----------------|--------|-----------------------------|-------------|--|
| Bits           | Access | Default                     | Field Name  | Description  |
| 31:0           |        | 0xFFFFFFFF                  | CcpPassword | CCP Password to protect CCP read/write actions via IO-Link - transmitted in ISDU 0x201 |

### 12.31.2 0xFE – CcpVersion

| Address : 0xFE |        | Register Name : CcpVersion |            | Default: 0x86000001     |
|----------------|--------|----------------------------|------------|-------------------------|
| Bits           | Access | Default                    | Field Name | Description             |
| 31:24          |        | 0x86                       | Pid        | Product specific CCP ID |
| 23:16          |        | 0x0                        | PatchVer   | Patch Version of CCP    |
| 15:8           |        | 0x0                        | MinorVer   | Minor Version of CCP    |
| 7:0            |        | 0x1                        | MajorVer   | Major Version of CCP    |

### 12.31.3 0xFF – CrcCcp1

Wrong setting of this parameter hinders firmware execution. Leave the computation of necessary setup for this register to the GUI.

| Address : 0xFF |        | Register Name : CrcCcp1 |            | Default: 0xD4F0D265 |
|----------------|--------|-------------------------|------------|---------------------|
| Bits           | Access | Default                 | Field Name | Description         |
| 31:0           |        | 0xD4F0D265              | CrcCcp1    | CRC of CCP Page 1   |

## 13 Application Information

### 13.1 2-Bridge Application 1.8V to 5.5V Supply

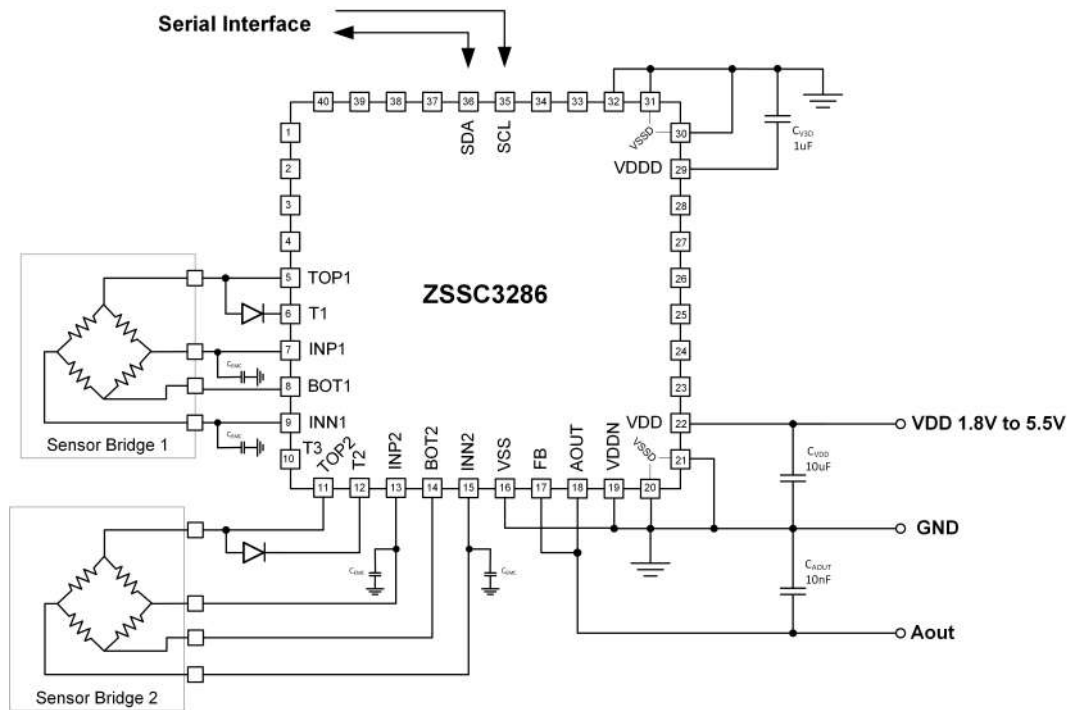


Figure 43: 2-Bridge Application 1.8V to 5.5V Supply

### 13.2 Single Bridge Application with IO-Link

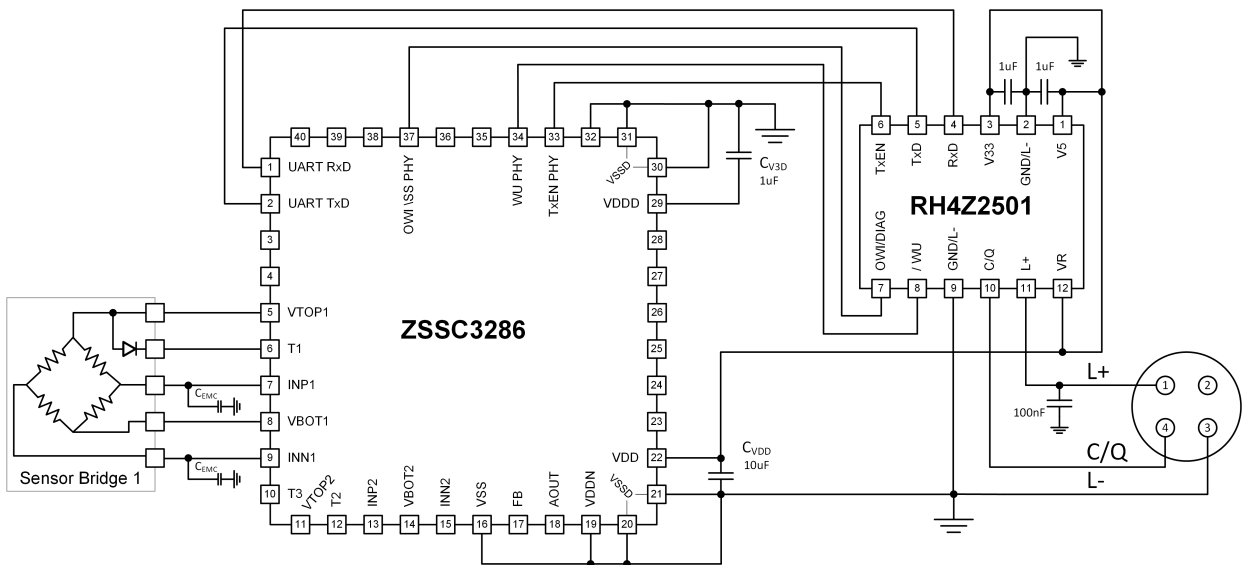


Figure 44: Single Bridge Application with IO-Link

### 13.3 Single Bridge Application with IO-Link and Current Loop Output

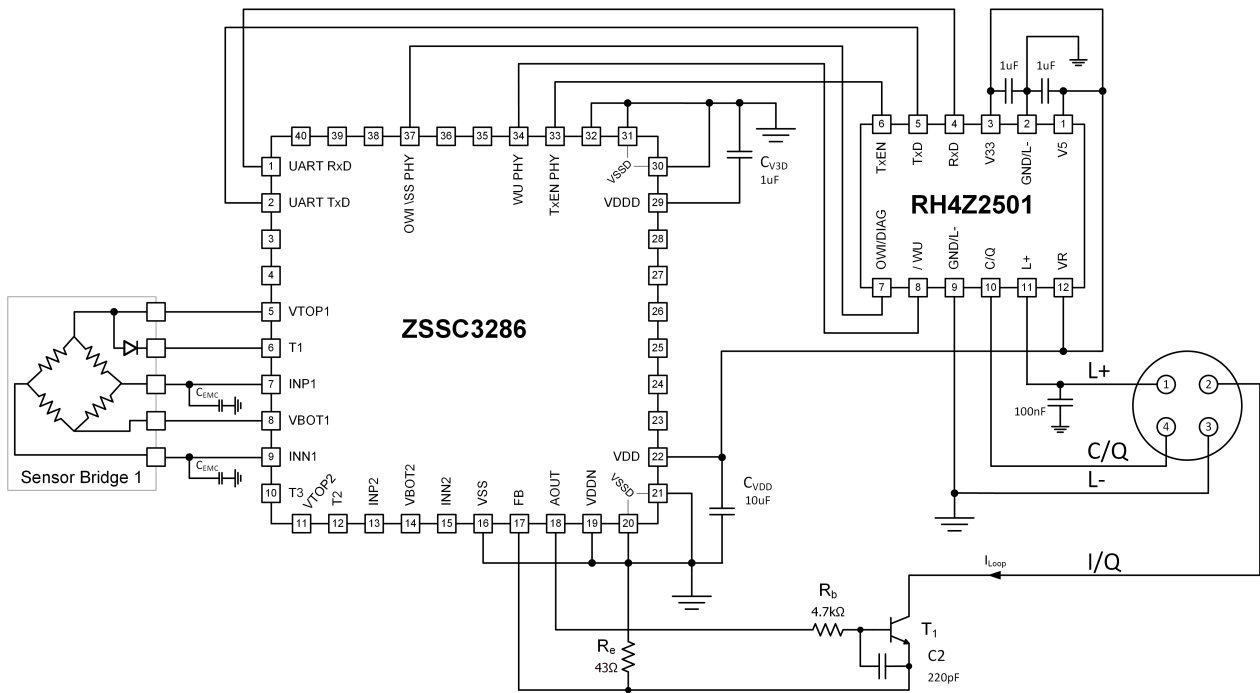


Figure 45: Single Bridge Application with IO-Link and Current Loop Output

## 14 Package Information

### 14.1 Package Outline Drawings

The package outline drawings are accessible from the link below. The package information is the most current data available.

[Package Outline Drawing Package Code: NDG40S1 40-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.4 mm Pitch \(renesas.com\)](#)

### 14.2 Marking Diagram



1. "ZSSC3286B" is the truncated part number.
2. "YyywwGR" where "Y" and "GR" are fixed and "yyww" represents the last digits of the year and week that the part was assembled.
3. "LOT" is the complete lot number of the part.

Figure 46: Marking Diagram



## 15 Glossary, References and History

### 15.1 Glossary

| Term | Description  |
|------|--|
| ADC  | Analog to Digital Converter  |
| AFE  | Analog Front End   |
| ARM  | Provider of microcontroller core                                     |
| AUX  | Auxiliary measurement, in addition to main sensor bridge measurement |
| AZ   | Auto-zero  |
| BLOB | Binary Large Object  |
| BOT  | Bottom   |
| CCP  | Configuration and Calibration Page                                   |
| DAC  | Digital to Analog Converter  |
| EMI  | Electromagnetic Interference   |
| ESD  | Electrostatic Discharge  |
| FB   | Feedback input for analog output buffer                              |
| FS   | Full Scale   |
| FW   | Firmware   |
| GPIO | General Purpose Input Output   |
| GUI  | Graphical User Interface   |
| HF   | High Frequency   |
| HW   | Hardware   |
| I2C  | Inter Integrated Circuit communication protocol                      |
| ID   | Identification   |
| IIR  | Infinite Impulse Response  |
| ISDU | Indexed Service Data Unit  |
| LDR  | Lower Diagnostic Range   |
| LF   | Low Frequency  |
| LSB  | Least Significant Bit  |
| MISO | Master-In Slave-Out  |
| MOSI | Master-Out Slave-In  |
| MSB  | Most Significant Bit   |
| OWI  | One Wire Interface   |
| PGA  | Programmable Gain Amplifier  |
| PHY  | Physical Layer   |
| POR  | Power-On-Reset   |
| PTAT | Proportional to absolute temperature current source                  |
| R    | Read   |
| RAM  | Random Access Memory   |
| RCA  | Renesas Code Area  |
| RDAC | Resistive Digital to Analog Converter                                |
| RTD  | Temperature dependent resistor                                       |
| RW   | Read/Write   |
| SM-  | Main Sensor Measurement, inverted signal polarity                    |
| SM+  | Main Sensor Measurement, standard (non-inverted) signal polarity     |
| SOT  | Second Order Term  |
| SPI  | Serial Peripheral Interface  |
| SS   | Slave Select   |
| SSC  | Sensor Signal Conditioner  |
| SSP  | Smart Sensor Profile   |

Continued on next page

| Term | Description                                   |
|------|---|
| TFW  | Fechnology Firmware                           |
| TLC  | Third Logic Channel                           |
| UART | Universal Asynchronous Receiver / Transmitter |
| UDR  | Upper Diagnostic Range                        |
| W    | Write   |
| WURQ | Wake-Up Request                               |

## 15.2 References

| Reference Number | Title  |
|------------------|--|
| 1                | IO-Link Interface and System. Specification. Version 1.1.3. June 2019                    |
| 2                | IO-Link Common Profile. Specification. Version 1.1. December 2021                        |
| 3                | RH4Z2501 <a href="https://www.renesas.com/RH4Z2501">https://www.renesas.com/RH4Z2501</a> |

## 15.3 Firmware Revision History

| Revision | Date          | Description     |
|----------|---------------|-----------------|
| 1.0.0    | July 31, 2024 | Initial release |

## 15.4 Document Revision History

| Revision | Date               | Description     |
|----------|--------------------|-----------------|
| 1.0      | September 18, 2024 | Initial release |