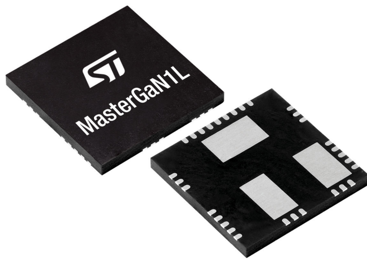
MASTERGAN1L

Datasheet

600 V half-bridge enhancement mode GaN HEMT with high voltage driver



Product status link
MASTERGAN1L

Product label

Features

- 600 V system-in-package integrating half-bridge gate driver and high-voltage power GaN transistors:
  - QFN 9 x 9 x 1 mm package
  - $R_{DS(ON)}$ = 150 mΩ
  - $I_{DS(MAX)}$ = 10 A
- Reverse current capability
- Zero reverse recovery loss
- UVLO protection on VCC
- Internal bootstrap diode
- Interlocking function
- Dedicated pin for shutdown functionality
- Accurate internal timing match
- 3.3 V to 15 V compatible inputs with hysteresis and pull-down
- Overtemperature protection
- Bill of material reduction
- Very compact and simplified layout
- Flexible, easy and fast design.

Application

- High frequency Resonant Converters including LLC, LCC and Resonant Flyback
- Active Clamp Flybacks
- Switch-mode power supplies
- Chargers and adapters
- PFC, High-voltage DC-DC and DC-AC Converters

Description

The MASTERGAN1L is an advanced power system-in-package integrating a gate driver and two enhancement mode GaN transistors in half-bridge configuration.

The integrated power GaNs have $R_{DS(ON)}$ of 150 mΩ, 650 V drain-source blocking voltage, while the high side of the embedded gate driver can be easily supplied by the integrated bootstrap diode.

The MASTERGAN1L features UVLO protection on VCC, preventing the power switches from operating in low efficiency or dangerous conditions, and the interlocking function avoids cross-conduction conditions.

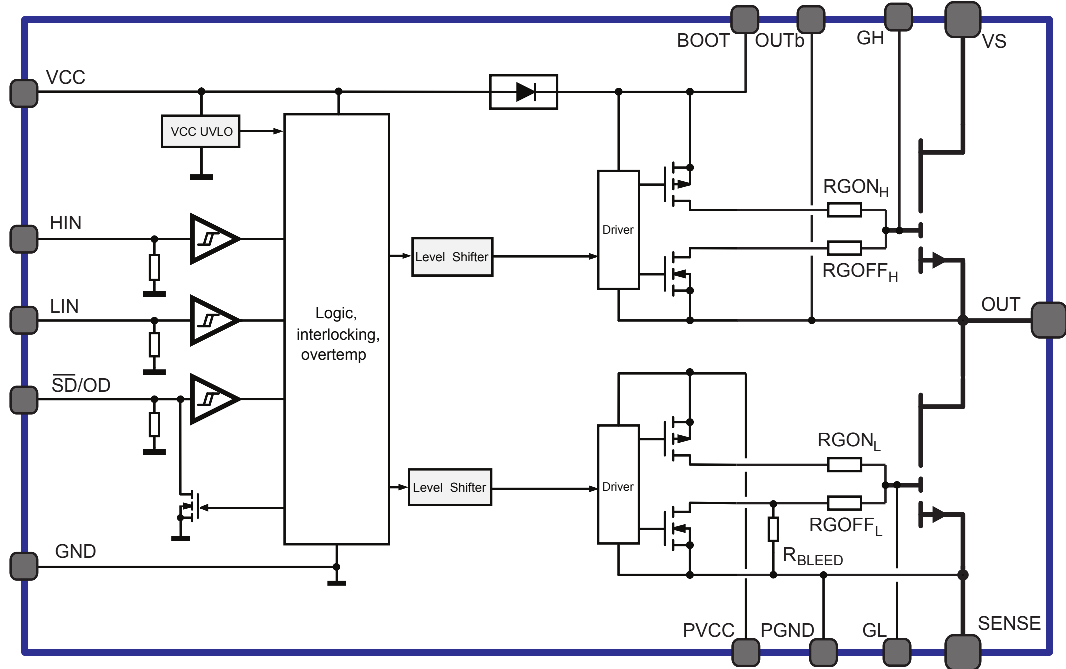
The input pins extended range allows easy interfacing with analog controllers, microcontrollers and DSP units.

The MASTERGAN1L operates in the industrial temperature range, -40°C to 125°C.

The device is available in a compact 9x9 mm QFN package.

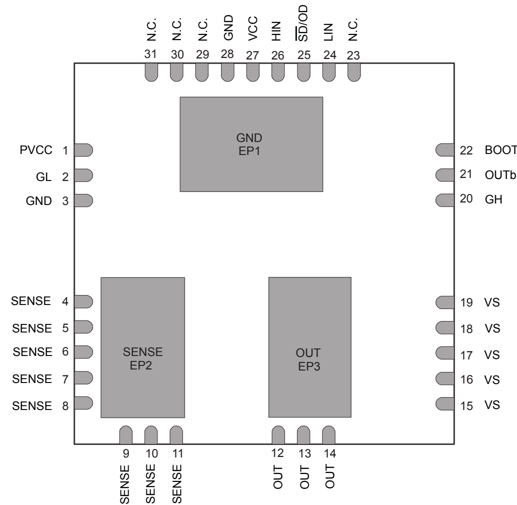
1 Block diagram

Figure 1. Block diagram



2 Pin description and connection diagram

Figure 2. Pin connection (top view)



2.1 Pin list

Table 1. Pin description

Pin Number	Pin Name	Type	Function
15, 16, 17, 18, 19	VS	Power Supply	High voltage supply (high-side GaN Drain)
12, 13, 14, EP3	OUT	Power Output	Half-bridge output
4, 5, 6, 7, 8, 9, 10, 11, EP2	SENSE	Power Supply	Half-bridge sense (low-side GaN Source)
22	BOOT	Power Supply	Gate driver high-side supply voltage
21	OUTb	Power Supply	Gate driver high-side reference voltage, used only for Bootstrap capacitor connection. Internally connected to OUT.
27	VCC	Power Supply	Logic supply voltage
1	PVCC	Power Supply	Gate driver low-side supply voltage
28, EP1	GND	Power Supply	Logic ground
3	PGND	Power Supply	Gate driver low-side driver reference. Internally connected to SENSE.
26	HIN	Logic Input	High-Side driver logic input
24	LIN	Logic Input	Low-Side driver logic input
25	$\overline{SD}$/OD	Logic Input-Output	Driver Shutdown input and Over-Temperature
2	GL	Output	Low-Side GaN gate.
20	GH	Output	High-Side GaN gate.
23, 29, 30, 31	N.C.	Not Connected	Leave floating

3 Electrical Data

3.1 Absolute maximum ratings

Table 2. **Absolute maximum ratings (each voltage referred to GND unless otherwise specified)**

Symbol	Parameter	Test Condition	Value	Unit
V_{DS}	GaN Drain-to-Source Voltage	T_J = 25 °C	620	V
I_D	Drain current	DC @ T_{CB} = 25°C ,[1] [2]	9.7	A
		DC @ T_{CB} = 100°C,[1] [2]	6.4	A
		Peak @ T_{CB} = 25°C [1], [2], [3]	17	A
VCC	Logic supply voltage		-0.3 to 11	V
PVCC-PGND	Low-side driver supply voltage [4]		-0.3 to 7	V
VCC-PGND	Logic supply vs. Low-side driver ground		-0.3 to 18.3	V
PVCC	Low-side driver supply vs. logic ground		-0.3 to 18.3	V
PGND	Low-side driver ground vs. logic ground		-7.3 to 11.3	V
V_{BO}	BOOT to OUTb voltage [5]		-0.3 to 7	V
BOOT	Bootstrap voltage		-0.3 to 620	V
$P_{RintGL(GH)}$	Maximum power dissipation of each set of internal driving resistances [6]	T_{CB} = 100°C	40	mW
S_{Rout}	Half-bridge outputs slew rate (10% - 90%)		100	V/ns
V_i	Logic inputs voltage range		-0.3 to 21	V
T_J	Junction temperature		-40 to 150	°C
T_s	Storage temperature		-40 to 150	°C

1. *T_{CB} is temperature of case exposed pad.*
2. *Range estimated by characterization, not tested in production.*
3. *Value specified by design factor, pulse duration limited to 50 µs and junction temperature.*
4. *PGND internally connected to SENSE.*
5. *OUTb internally connected to OUT.*
6. *See Section 5.3*

3.2 Recommended operating conditions

Table 3. Recommended operating conditions (Each voltage referred to GND unless otherwise specified)

Symbol	Parameter	Note	Min	Max	Unit
VS	High voltage bus		0	520	V
VCC	Supply voltage		4.75	9.5	V
PVCC-PGND	PVCC to PGND low side supply [1]		4.75	6.5	V
		Best performance	5	6.5	V
PVCC	Low-side driver supply		3	8.5	V
VCC-PVCC	VCC to PVCC pin voltage		-3	3	V
PGND	Low-side driver ground[1]		-2	2	V
DT	Suggested minimum deadtime		10		ns
T_{ON_MIN}	Suggested minimum Pulse duration		50		ns
T_{OFF_MIN}	Suggested minimum Negative Pulse duration	LIN	50		ns
		HIN	120		ns
V_{BO}	BOOT to OUTb pin voltage[2]		4.4	6.5	V
		Best performance	5	6.5	V
BOOT	BOOT to GND voltage		0[3]	530	V
V_i	Logic inputs voltage range		0	20	V
T_J	Junction temperature		-40	125	°C

1. *PGND internally connected to SENSE.*
2. *OUTb internally connected to OUT.*
3. *5 V is recommended during high-side turn-on.*

3.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(J-CB)}$	Thermal resistance junction to each GaN transistor exposed pad, typical	1.9	°C/W
$R_{th(J-A)}$	Thermal resistance junction-to-ambient[1]	17.5	°C/W

1. *The junction to ambient thermal resistance is obtained simulating the device mounted on a 2s2p (4 layer) FR4 board as JESD51-5,7 with 6 thermal vias for each exposed pad. Power dissipation uniformly distributed over the two GaN transistors.*

4 Electrical characteristics

Table 5. Driver electrical characteristics: VCC = PVCC = 6 V; SENSE = GND; T_J = 25 °C, unless otherwise specified.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
GaN Characteristics						
$V_{(BR)DS}$	Drain-source blocking voltage (1)	I_{DSS} < 18 µA(2) V_{GS} = 0 V	650			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 600 V V_{GS} = 0 V		0.7		µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 2.5 mA (2)		1.7		V
I_{GS}	Gate to source current	V_{DS} = 0 V (3)		30		µA
$R_{DS(on)}$	Static drain-source on-resistance	I_D = 3.2 A, T_J = 25°C		150	220	mΩ
$R_{DS(on)}$	Static drain-source on-resistance	I_D = 3.2 A, T_J = 125°C (3)		330		mΩ
Q_G	Total gate charge	V_{GS} = 6 V, T_J = 25 °C V_{DS} = 0 to 400 V (4)		2		nC
Q_{OSS}	Output charge	V_{GS} = 0 V, V_{DS} = 400 V (4)		20		nC
E_{OSS}	Output Capacitance stored energy	V_{GS} = 0 V, V_{DS} = 400 V (4)		2.7		µJ
C_{OSS}	Output capacitance	V_{GS} = 0 V, V_{DS} = 400 V (4)		20		pF
$C_{O(ER)}$	Effective output capacitance energy related (5)	V_{GS} = 0 V, V_{DS} = 0 to 400 V (4)		31		pF
$C_{O(TR)}$	Effective output capacitance time related (6)	V_{GS} = 0 V, V_{DS} = 0 to 400 V (4)		50		pF
E_{on}	Turn-on switching losses	(4)		12.5		µJ
E_{off}	Turn-off switching losses	(4)		2.5		µJ
Q_{RR}	Reverse recovery charge			0		nC
I_{RRM}	Reverse recovery current			0		A
$t_{C(on)}$	Crossover time (on)	VS = 400 V, VGS = 6 V, ID = 3.2 A See Figure 3(4)		15		ns
$t_{C(off)}$	Crossover time (off)	VS = 400 V, VGS = 6 V, ID = 3.2 A See Figure 3(4)		15		ns
td_{SD}	Shutdown to high/low-side propagation delay			70		ns
T_{d_GL}	LIN to GL propagation delay	See Figure 3 (2)		45		ns
T_{d_GH}	HIN to GH propagation delay	See Figure 3 (2)		45		ns
Logic section supply (Voltages referred to GND unless otherwise specified)						
VCC_{thON}	VCC UV turn ON threshold		4.2	4.5	4.75	V
VCC_{thOFF}	VCC UV turn OFF threshold		3.9	4.2	4.5	V
VCC_{hys}	VCC UV hysteresis		0.2	0.3	0.45	V
I_{QVCCU}	VCC undervoltage quiescent supply current	VCC = PVCC = 3.8 V		320	410	µA
I_{QVCC}	VCC quiescent supply current	$\overline{SD}$/OD = LIN = 5 V; HIN = 0 V; BOOT = 7 V		680	900	µA
I_{SVCC}	VCC switching supply current	$\overline{SD}$/OD = 5 V; V_{BO} = 6.5 V; VS = 0 V; F_{SW} = 500 kHz		0.8		mA
Low-side driver section supply (Voltages referred to PGND unless otherwise specified)						
I_{QPVCC}	PVCC quiescent supply current	$\overline{SD}$/OD = LIN = 5 V		150		µA

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{QPVCC}	PVCC quiescent supply current	$\overline{SD}$/OD = 5 V; LIN = 0V		0		µA
I_{SPVCC}	PVCC switching supply current	VS = 0 V F_{SW} = 500 kHz		1.4		mA
R_{BLEED}	Low side gate bleeder	PVCC = PGND	75	100	125	kΩ
RON_L	Low side turn on resistor			50		Ω
$ROFF_L$	Low side turn off resistor			2		Ω
High-side floating section supply (Voltages referred to OUTb unless otherwise specified)						
I_{QBO}	V_{BO} quiescent supply current [7]	V_{BO} = 6 V; LIN = GND; $\overline{SD}$/OD = HIN = 5 V;		50		µA
		V_{BO} = 6 V; LIN = HIN = GND; $\overline{SD}$/OD = 5 V; VBOOT = 11 V		0		µA
I_{SBO}	V_{BO} switching supply current [7]	V_{BO} =6 V; $\overline{SD}$/OD = 5 V; VS = 0 V; F_{SW} = 500 kHz		1.4		mA
I_{LK}	High voltage leakage current	BOOT = OUT = 600 V			11	µA
R_{DBoot}	Bootstrap diode on resistance [8]	$\overline{SD}$/OD = LIN = 5 V; HIN = GND = PGND VCC – BOOT = 0.5 V		140	175	Ω
RON_H	High side turn on resistor			50		Ω
$ROFF_H$	High side turn off resistor			2		Ω
Logic inputs						
V_{il}	Low level logic threshold voltage	T_J = 25 °C	1.1	1.31	1.45	V
		Full Temperature range [3]	0.8			
V_{ih}	High level logic threshold voltage	T_J = 25 °C	2	2.17	2.5	V
		Full Temperature range [3]			2.7	
V_{ihys}	Logic input threshold hysteresis		0.7	0.96	1.2	V
I_{INh}	Logic ‘1’ input bias current	LIN, HIN = 5 V	23	33	55	µA
I_{INl}	Logic ‘0’ input bias current	LIN, HIN = GND			1	µA
R_{PD_IN}	Input pull-down resistor	LIN, HIN = 5 V	90	150	220	kΩ
Shut Down ($\overline{SD}$/OD) pin						
I_{SDh}	Logic “1” input bias current	$\overline{SD}$/OD = 5 V	11	15	20	µA
I_{SDl}	Logic “0” input bias current	$\overline{SD}$/OD = 0 V			1	µA
R_{PD_SD}	Pull-down resistor	$\overline{SD}$/OD = 5 V OpenDrain OFF	250	330	450	kΩ
V_{TSD}	Thermal shutdown unlatch threshold	T_J = 25 °C [2]	0.5	0.75	1	V
R_{ON_OD}	Open drain ON resistance	T_J = 25 °C; I_{OD} = 400 mV [2]	8	10	18	Ω
I_{OL_OD}	Open Drain low level sink current	T_J = 25 °C; V_{OD} = 400 mV [2]	22	40	50	mA
Over temperature protection						
T_{TSD}	Shut down temperature	[3]		175		°C
T_{HYS}	Temperature Hysteresis	[3]		20		°C

1. *Transistor Blocking voltage is measured between VS pin and OUT pin. OUT pin voltage rating is defined by BOOT pin rating.*
2. *Tested on wafer*
3. *Range estimated by characterization, not tested in production.*
4. *Typical values based on characterization and simulations: not tested in production.*

5. $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy while V_{DS} is rising from 0 V to the stated V_{DS}
6. $C_{O(TR)}$ is the fixed capacitance that would give the same charging time while V_{DS} is rising from 0 V to the stated V_{DS}
7. $V_{BO} = V_{BOOT} - V_{OUT}$
8. $R_{DBoot(on)}$ is tested in the following way

   $R_{DBoot(on)} = [(VCC - V_{BOOTa}) - (VCC - V_{BOOTb})] / [I_a - I_b]$

   Where: I_a is BOOT pin current when $V_{BOOT} = V_{BOOTa}$; I_b is BOOT pin current when $V_{BOOT} = V_{BOOTb}$

Figure 3. Switching time definition

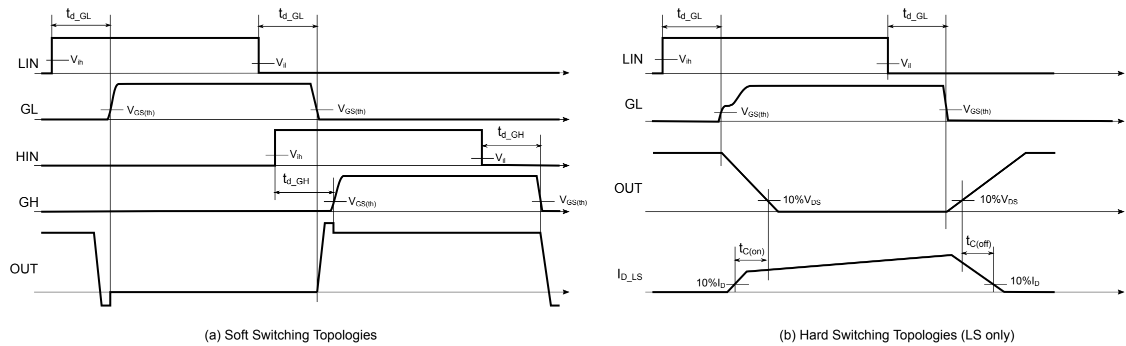


Figure 4. Typ I_D vs. V_{DS} at T_J = 25 °C

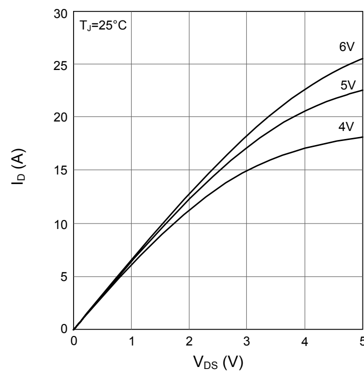


Figure 5. Typ I_D vs. V_{DS} at T_J = 125 °C

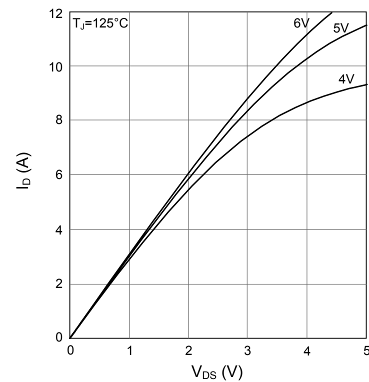


Figure 6. Typ $R_{DS(on)}$ vs. I_D at T_J = 25 °C

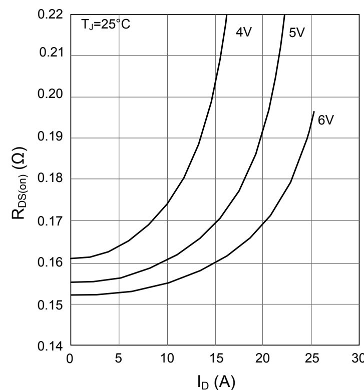


Figure 7. Typ $R_{DS(on)}$ vs. I_D at T_J = 125 °C

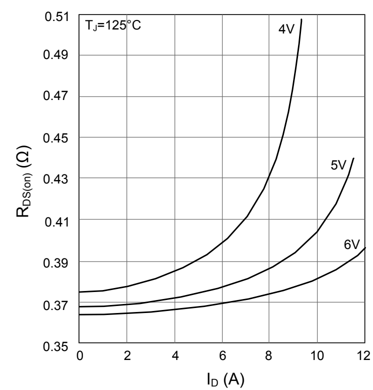


Figure 8. Typ I_D vs. V_{DS}

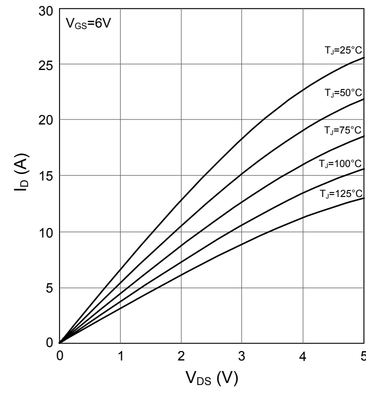


Figure 9. Typ $R_{DS(on)}$ vs. T_J, normalized at 25°C

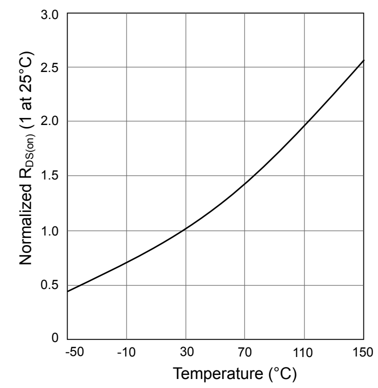


Figure 10. Typ I_{SD} vs. V_{SD}, at T_J = 25 °C

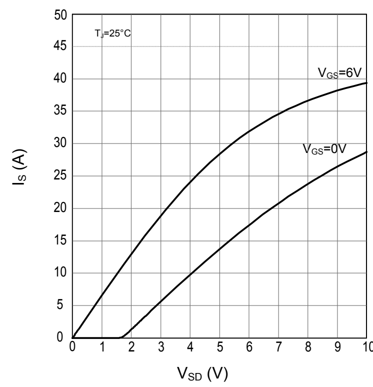


Figure 11. Typ I_{SD} vs. V_{SD}, at T_J = 125 °C

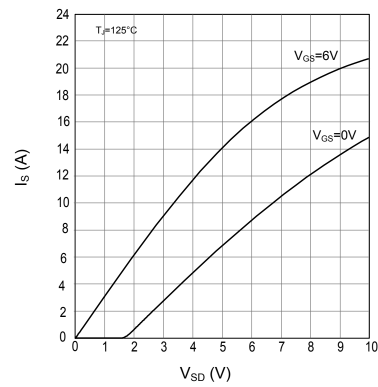


Figure 12. Safe Operating Area at T_J = 25 °C

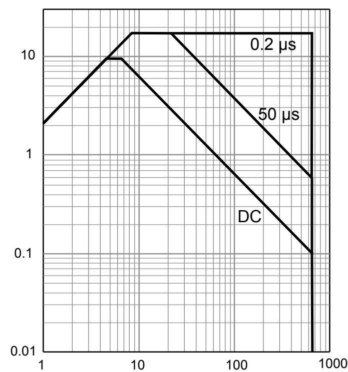


Figure 13. Derating curve

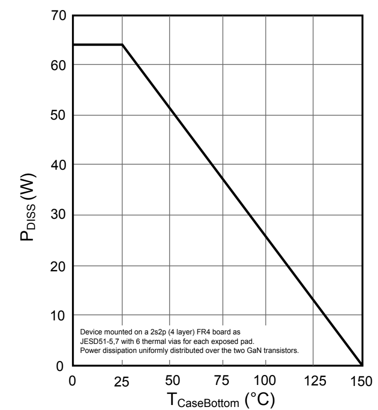


Figure 14. Typ Gate Charge at T_J = 25 °C

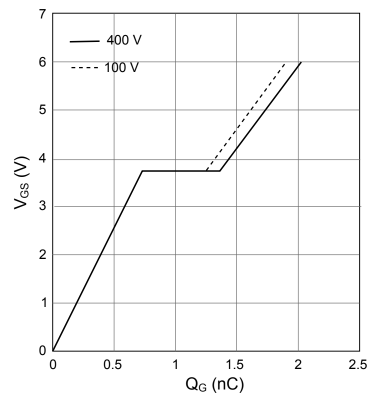
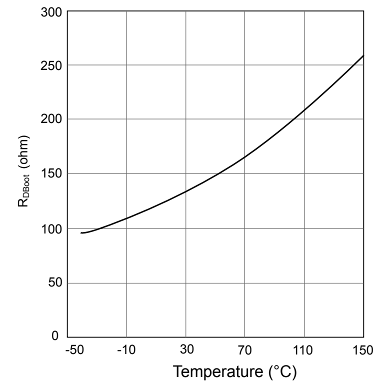


Figure 15. Typ R_{Dboot} vs T_J



5 Functional description

5.1 GaN transistor

The MASTERGAN1L embeds two 650 V enhanced mode GaN transistors, connected in half-bridge configuration. The technology of the embedded GaN transistors does not need bipolar driving: for this reason, negative voltage to turn off the transistor is not necessary.

The low-side GaN transistor is electrically connected between the OUT pin set (drain) and SENSE pin set (source): the SENSE exposed pad also represents a thermal buffer for this transistor. A suitable copper area and several thermal vias are required to dissipate the power losses generated during normal operation.

The maximum voltage applicable between drain and source of this GaN transistor is defined (statically and dynamically) by the maximum voltage applicable between the floating reference of the integrated driver (approximately the OUT pin set) and ground.

The high-side GaN transistor is electrically connected between VS pins (drain) and OUT pins (source): the OUT exposed pad also represents a thermal buffer for this transistor. As suggested for low-side connection, a suitable copper area and several thermal vias are required to dissipate the power losses generated during normal operation.

The maximum voltage applicable between drain and source of this GaN transistor is equal to 650 V and is defined as the DC blocking voltage that causes the Drain to Source Leakage Current (I_{DSS}) to be higher than a defined limit in worst-case conditions (thermal and ageing). A 750 V pulse can be applied obtaining the same ageing effect, whilst the worst case non-recoverable breakdown voltage is approximately equal to 30% of blocking voltage (~845 V): this voltage has a negative thermal trend (worst-case occurs at T_J = 150 °C).

5.2 Design recommendations for a safe driver operation

The embedded GaN transistors do not have an intrinsic body diode and, consequently, exhibit zero reverse recovery losses. Nevertheless, the reverse conduction is permitted both during on state (in this case the V_{SD} drop is obtained by ohm's law applied to GaN's $R_{DSon)}$) and during off state (in this case the V_{SD} drop is obtained by a reverse conduction drop described in GaN's V_{SD} graph). Anti-parallel diodes are not required for proper functionality of MASTERGAN1L in both resonant and hard switching, but are recommended in resonant applications to maximize the efficiency, minimizing the reverse conduction period during deadtimes.

Every time the low-side switch current flows from source to drain a negative voltage drop (V_{SD}) appears on the OUT pin. This voltage is added to the bootstrap voltage of the high-side GaN causing an excess of voltage on the high-side gate that, if not properly manged, may overcome the gate maximum limit.
For a safe operating condition in every applicative environment, it is recommended to protect the gate of high-side GaN by adding a 6.8 V typ. Zener diode between the GH and OUTb pin . In Figure 19 , Figure 20 and Figure 21 a safe design of, respectively, an LLC ACF and Resonant Flyback are reported with a Zener diode properly placed.

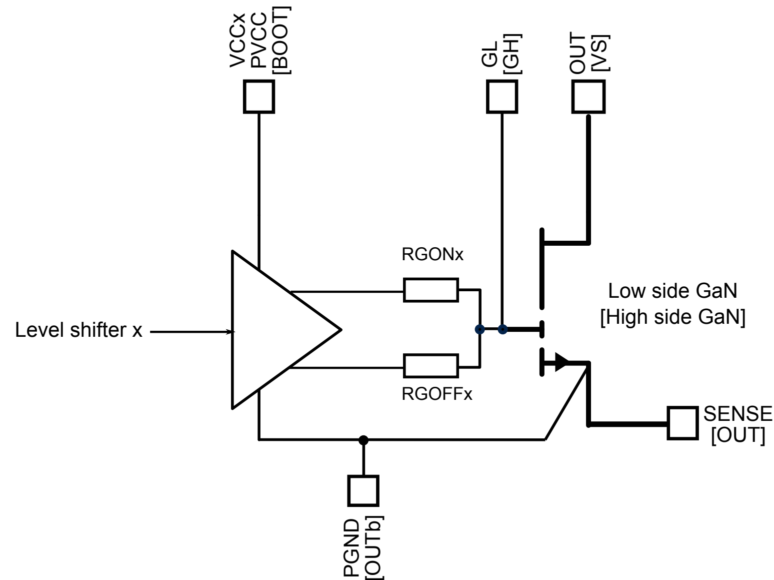
Design noise immunity of the final converter is also improved.

5.3 Internal driving resistors dissipation

The driver output stage acts between the gate and Kelvin source of the GaN transistor: positive voltage turns the GaN on while zero voltage turns the GaN off.

Turn-on and turn-off resistors (RG_{ON} and RG_{OFF}) required to control the switching speed and slew rate are already fixed internally. The turn-on internal resistance (RG_{ONx}) is tailored on the GaN transistor's characteristics.

Figure 16. Internal driving resistors configuration



The delay to on-times and the delay to off-times is determined by the sum of the propagation delays of the Drivers and turn-on time of the used GaN transistors.

In some circumstances, external pull-down resistors and external capacitors can be connected between GL and PGND or GH and OUTb. The maximum attachable load, C_{LOAD} and R_{LOAD}, must not surpass the maximum power rating of internal resistances, that equals:

Equation 2

$$P_{LOSS,RGON} = VCCx^2 \cdot \left[\left(\frac{Q_G}{VCCx} + C_{LOAD}\right) \cdot f_{sw} + \left(\frac{RGONx}{(RGONx + R_{LOAD})^2}\right) \cdot \delta_C\right] \quad (2)$$

Where f_{sw} represents the switching frequency and δ_C is the duty cycle of the side under consideration.

5.4 Logic inputs

The device features a half-bridge gate driver with three logic inputs to control the internal high-side and low-side GaN transistors.

The devices are controlled through the following logic inputs:

- $\overline{SD}$/OD: Shutdown input, active low;
- LIN: low-side driver inputs, active high;
- HIN: high-side driver inputs, active high.

Table 6. Inputs truth table (applicable when device is not in UVLO)

Input pins			GaN transistors status	
$\overline{SD}$/OD	LIN	HIN	LS	HS
L	X(1)	X(1)	OFF	OFF
H	L	L	OFF	OFF
H	L	H	OFF	**ON**
H	H	L	**ON**	OFF
H	H(2)	H(2)	OFF	OFF

1. *X: Don't care*
2. *Interlocking*

The logic inputs have internal pull-down resistors. The purpose of these resistors is to set a proper logic level in case, for example, there is an interruption in the logic lines or the controller outputs are in tri-state conditions.

If logic inputs are left floating, the gate driver outputs are set to low level and the correspondent GaN transistors are turned off.

The minimum recommended duration of the on time of the signal applied to LIN or HIN is T_{ON_MIN} = 50 ns; shorter pulses could be either distorted or blanked.

The minimum duration of the off time of the signal applied to LIN and HIN is respectively T_{OFF_MIN} = 50 ns and T_{OFF_MIN} = 120 ns; shorter off times shall be either extended to T_{OFF_MIN} or blanked.

Interlocking feature shuts down both transistor to avoid unexpected cross-conduction if LIN and HIN are simultaneously high.

5.5 Bootstrap structure

The device integrates a bootstrap circuit to charge the capacitor that supplies the high voltage section (C_{BOOT}) reducing the external components.

The bootstrap integrated circuit is connected to the VCC pin and is driven synchronously with the low-side driver.

The minimum value of the bootstrap capacitor is selected to ensure that the high-side driver supply voltage (V_{BO}) remains within the recommended operating range (suggested VBO_{ripple} = 250 mV). Larger values of C_{BOOT} ensure cleaner V_{BO}, increase the hold up time, but require longer time to wake up the MASTERGAN.

Equation 1

$$C_{Boot,min} \geq \frac{Q_{BO}}{VBO_{ripple}} \quad (1)$$

Where

Equation 2

$$Q_{BO} = Q_G + I_{qBO@HINon} \cdot \frac{\delta_{HS}}{f_{sw}} + I_{LK} \cdot \frac{(1 - \delta_{LS})}{f_{sw}} + \frac{I_{qBO@HINoff}}{f_{sw}} \quad (2)$$

Equation 3

$$VBO_{ripple} = VCC - V_{F_{Dboot}} - VBO_{min} \quad (3)$$

The value of V_{FDboot} can be considered equal to zero when the internal bootstrap structure is used, while δ_{LS} and δ_{HS} are the operating duty cycles of the low-side GaN and high-side GaN.

The series resistance of the internal bootstrap circuit limits both the charging current and the charging time.

The average bootstrap voltage is obtained by the balance between the average charging current ($I_{DbootCH_avg}$) and high-side driver consumption (I_{SBO}). The typical value of the latter quantity depends linearly on the switching frequency with a contribution approximately equal to 2.8 μA/kHz.

Equation 4

$$I_{DbootCH_avg} \sim \frac{\left(VCC - VBO_{avg}\right)}{\frac{R_{DBoot}}{\delta_{LS,\,min}}} \tag{4}$$

Equation 5

$$VBO_{avg} = VCC - \frac{I_{SBO} \cdot R_{DBoot}}{\delta_{LS,\,min}} \sim VCC - \frac{fsw \cdot 2.8\frac{\mu A}{kHz} \cdot R_{DBoot}}{\delta_{LS,\,min}} \tag{5}$$

If preliminary evaluation of VBO_{avg} leads to an insufficient value, an external bootstrap diode is required. The series of an ultrafast 600 V / 1 A diode with proper series resistance is recommended (STTH1L06 or equivalent). The series resistance value should be selected between a maximum value that guarantee a sufficient VBO_{avg} and a minimum value that ensures an initial charging time (V_{BO} > 4.5 V) that satisfies the application constraints.

Equation 6

$$T_{Charging} > R_{DBoot} \cdot C_{Boot} \tag{6}$$

5.6 VCC supply pins and UVLO function

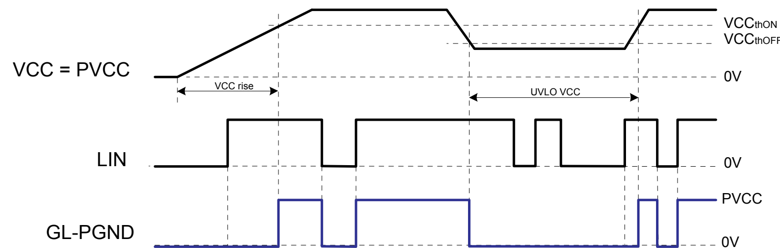
The VCC pin supplies current to the logic circuit, level-shifters in the low-side section and the integrated bootstrap diode.

The PVCC pin supplies low-side output buffer. During output commutations the average current used to provide gate charge to the high-side and low-side GaN transistors flows through this pin.

The PVCC pin can be connected either to the same supply voltage of the VCC pin or to a separated voltage source. In case the same voltage source is used, it is suggested to connect VCC and PVCC pins by means of a small decoupling resistance. The use of dedicated bypass ceramic capacitors located as close as possible to each supply pin is highly recommended.

The VCC supply voltage is continuously monitored by an under-voltage lockout (UVLO) circuitry that turns both the high-side and low-side GaN transistors off when the supply voltage goes below the V_{CC_thOFF} threshold. The UVLO circuitry turns on the GaN, according to LIN and HIN status, as soon as the supply voltage goes above the V_{CCthON} voltage. A V_{CChys} hysteresis is provided for noise rejection purpose.

Figure 17. VCC UVLO and Low Side



5.7 Thermal shutdown

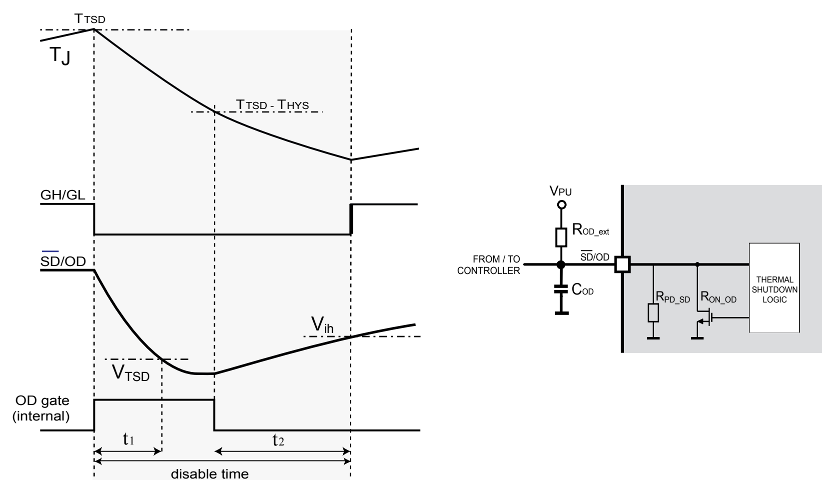
The integrated gate driver has a thermal shutdown protection.

When junction temperature reaches the T_{TSD} temperature threshold, the device turns off both GaN transistors leaving the half-bridge in 3-state and signaling the state forcing $\overline{SD}$/OD pin low. $\overline{SD}$/OD pin is released when junction temperature is below T_{TSD}-T_{HYS} and $\overline{SD}$/OD is below V_{TSD}.

GaN are driven again according to inputs when $\overline{SD}$/OD rises above V_{ih}.

The thermal smart shutdown system gives the possibility to increase the time constant of the external RC network (that determines the disable time after the over-temperature event) up to very large values without delaying the protection.

Figure 18. Thermal shutdown timing waveform



6 Typical application diagrams

Figure 19. Typical application diagram – Resonant LLC converter

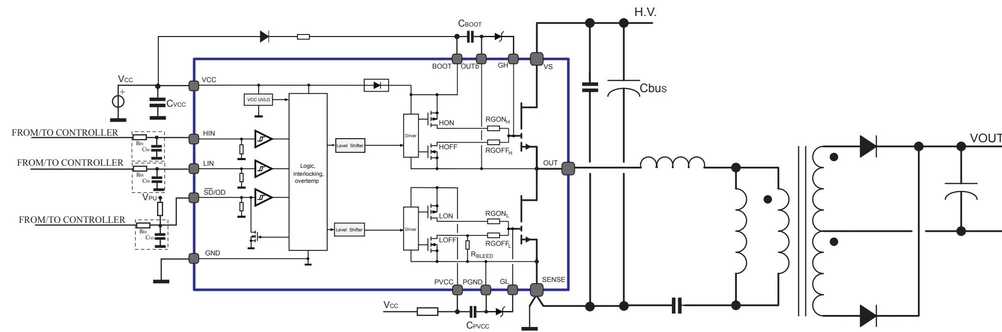


Figure 20. Typical application diagram – Active clamp flyback

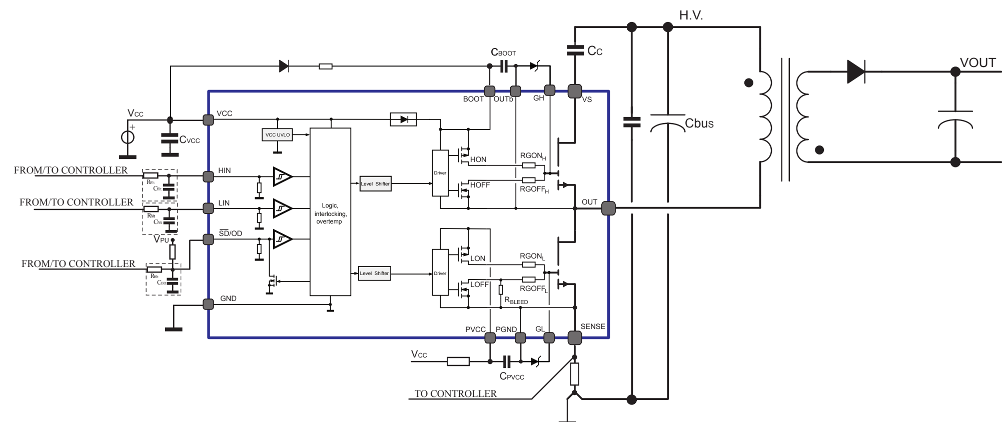
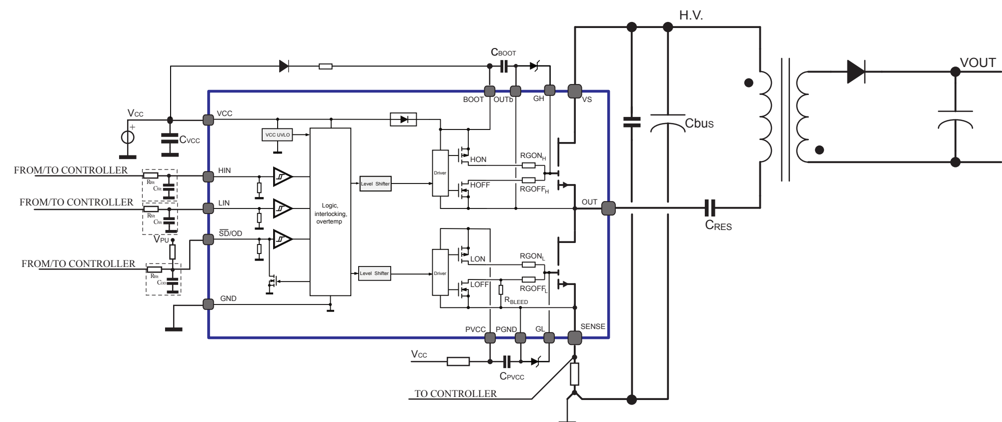


Figure 21. Typical Application diagram - Resonant flyback



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

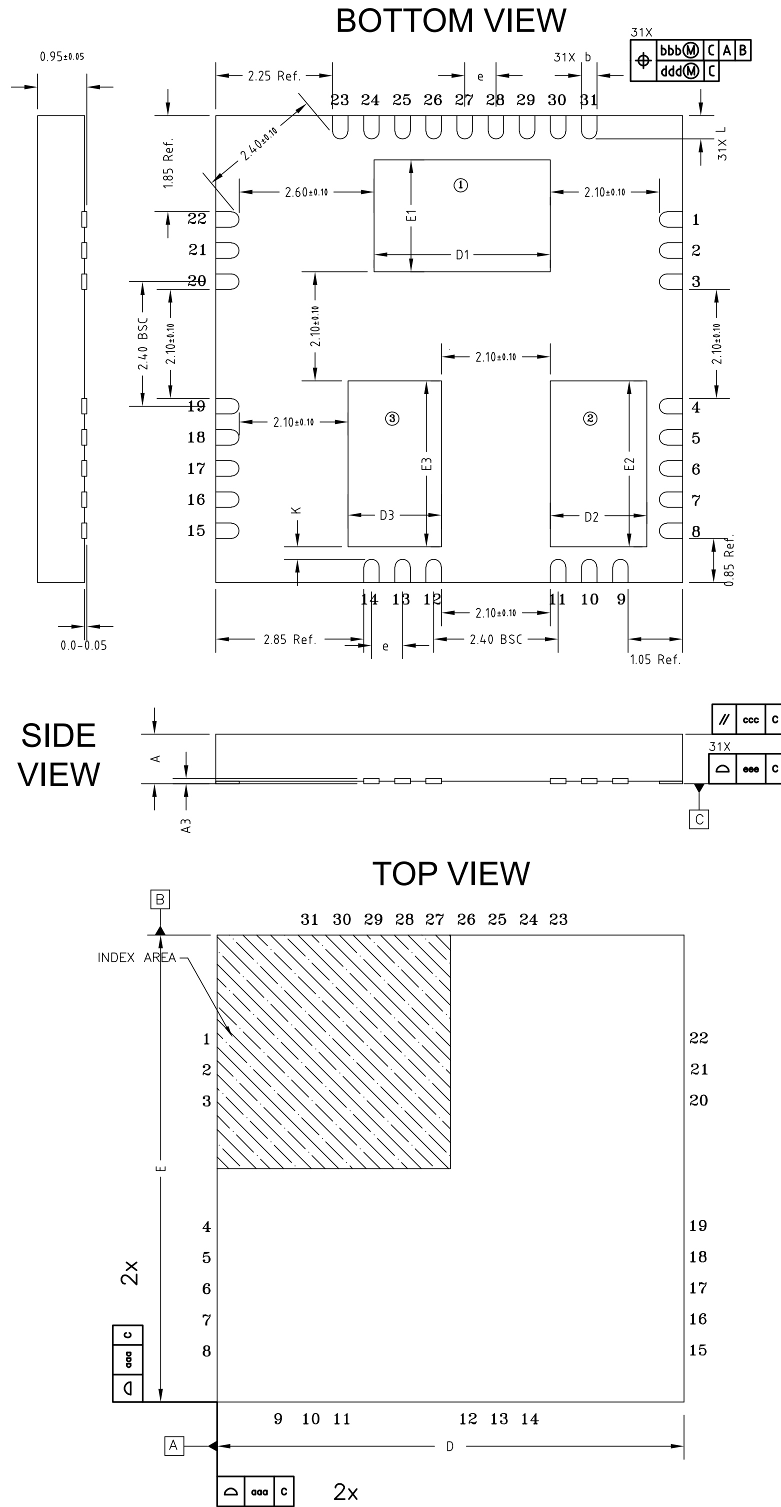
7.1 QFN 9 x 9 x 1 mm, 31 leads, pitch 0.6 mm package information

Table 7. QFN 9 x 9 x 1 mm package dimensions

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A3		0.10	
b	0.25	0.30	0.35
D	8.96	9.00	9.04
E	8.96	9.00	9.04
D1	3.30	3.40	3.50
E1	2.06	2.16	2.26
D2	1.76	1.86	1.96
E2	3.10	3.20	3.30
D3	1.70	1.80	1.90
E3	3.10	3.20	3.30
e		0.60	
K		0.24	
L	0.35	0.45	0.55
N	31		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:
1. *Dimensioning and tolerances conform to ASME Y14.5-2009.*
2. *All dimensions are in millimeters.*
3. *N total number of terminals.*
4. *Dimensions do not include mold protrusion, not to exceed 0.15 mm.*
5. *Package outline exclusive of metal burr dimensions.*

Figure 22. QFN 9 x 9 x 1 mm package dimensions

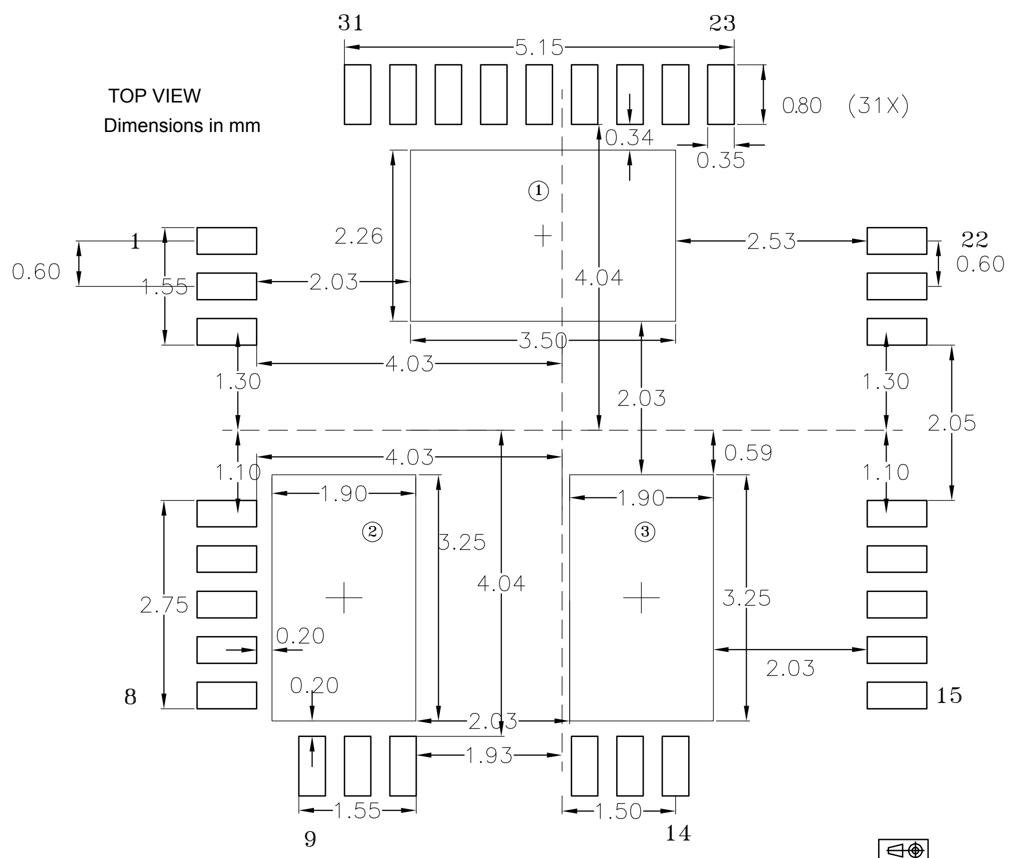


8 Suggested footprint

The suggested footprint for the PCB layout is usually defined based on several design factors such as assembly plant technology capabilities and board component density. For easy device usage and evaluation, ST provides the following footprint design, which is suitable for the largest variety of PCBs.

The following footprint indicates the copper area which should be free from the solder mask, while the copper area shall extend beyond the indicated areas especially for EP2 and EP3. To aid thermal dissipation, it is recommended to add thermal vias under these EPADs to transfer and dissipate device heat to the other PCB copper layers.

Figure 23. Suggested footprint (top view drawing)



9 Ordering information

Table 8. Order codes

Order code	Package	Package Marking	Packaging
MASTERGAN1L	QFN 9 x 9 x 1 mm	MASTERGAN1L	Tray
MASTERGAN1LTR	QFN 9 x 9 x 1 mm	MASTERGAN1L	Tape and Reel

Revision history

Table 9. **Document revision history**

Date	Version	Changes
07-Jul-2023	1	Initial release.

Contents

1 **Block diagram** 2
2 **Pin description and connection diagram** 3
2.1 Pin list 3
3 **Electrical Data** 4
3.1 Absolute maximum ratings 4
3.2 Recommended operating conditions 5
3.3 Thermal data 5
4 **Electrical characteristics** 6
5 **Functional description** 11
5.1 GaN transistor 11
5.2 Design recommendations for a safe driver operation 11
5.3 **Internal driving resistors dissipation** 11
5.4 Logic inputs 13
5.5 Bootstrap structure 13
5.6 VCC supply pins and UVLO function 15
5.7 Thermal shutdown 16
6 **Typical application diagrams** 17
7 **Package information** 18
7.1 QFN 9 x 9 x 1 mm, 31 leads, pitch 0.6 mm package information 18
8 **Suggested footprint** 20
9 **Ordering information** 21
Revision history 22
List of tables 24
List of figures 25

List of tables

Table 1. Pin description . . . 3
Table 2. Absolute maximum ratings (each voltage referred to GND unless otherwise specified) . . . 4
Table 3. Recommended operating conditions (Each voltage referred to GND unless otherwise specified) . . . 5
Table 4. Thermal data . . . 5
Table 5. Driver electrical characteristics: VCC = PVCC = 6 V; SENSE = GND; T_J = 25 °C, unless otherwise specified. . . . 6
Table 6. Inputs truth table (applicable when device is not in UVLO) . . . 13
Table 7. QFN 9 x 9 x 1 mm package dimensions . . . 18
Table 8. Order codes . . . 21
Table 9. Document revision history . . . 22

List of figures

Figure 1. Block diagram . . . 2
Figure 2. Pin connection (top view) . . . 3
Figure 3. Switching time definition . . . 8
Figure 4. Typ I_D vs. V_{DS} at T_J = 25 °C . . . 8
Figure 5. Typ I_D vs. V_{DS} at T_J = 125 °C . . . 8
Figure 6. Typ $R_{DS(on)}$ vs. I_D at T_J = 25 °C . . . 8
Figure 7. Typ $R_{DS(on)}$ vs. I_D at T_J = 125 °C . . . 8
Figure 8. Typ I_D vs. V_{DS} . . . 9
Figure 9. Typ $R_{DS(on)}$ vs. $T_{J,}$ normalized at 25°C . . . 9
Figure 10. Typ I_{SD} vs. V_{SD}, at T_J = 25 °C . . . 9
Figure 11. Typ I_{SD} vs. V_{SD}, at T_J = 125 °C . . . 9
Figure 12. Safe Operating Area at T_J = 25 °C . . . 9
Figure 13. Derating curve . . . 9
Figure 14. Typ Gate Charge at T_J = 25 °C . . . 10
Figure 15. Typ R_{Dboot} vs T_J . . . 10
Figure 16. Internal driving resistors configuration . . . 12
Figure 17. VCC UVLO and Low Side . . . 15
Figure 18. Thermal shutdown timing waveform . . . 16
Figure 19. Typical application diagram – Resonant LLC converter . . . 17
Figure 20. Typical application diagram – Active clamp flyback . . . 17
Figure 21. Typical Application diagram - Resonant flyback . . . 17
Figure 22. QFN 9 x 9 x 1 mm package dimensions . . . 19
Figure 23. Suggested footprint (top view drawing) . . . 20

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved