

Single-phase Full-wave Gate Driver IC for Fan Motor

KA44370A Datasheet

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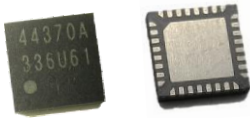
Functional safety standards for automobiles ISO26262	No
AEC-Q100	No
Market failure rate	50 Fit

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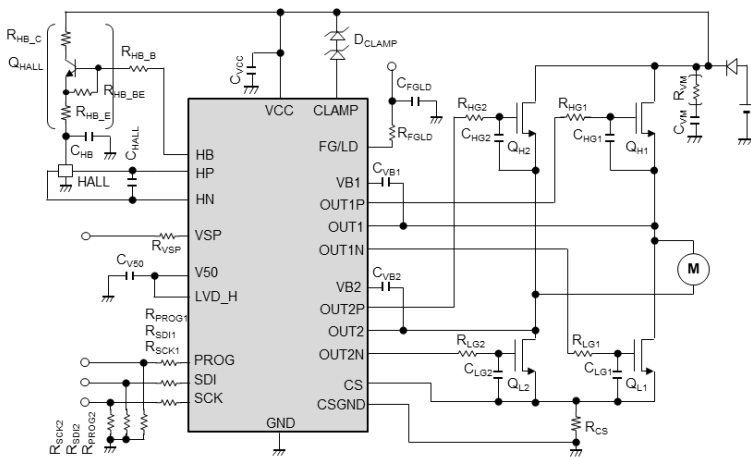
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FEATURES

- Supply voltage range : 8.0V ~ 76 V
 - Gate Driver for single-phase Motor (Nch / Nch MOS FET driving)
 - Advanced phase function and Soft switching make high efficiency and silent driving.
 - Optimal parameter can be set for various applications by writing to memory.
- Speed feedback control, Advanced phase, Motor lock protection time etc.
- Supports speed control using PWM / DC input.
 - FG pulse or LD (Motor lock detection) output can be selected.
 - Various protection functions.
Undervoltage lock out (UVLO), Thermal protection, Motor output current limiter, Motor lock detection.
 - QFN 32pin (4.0mm x 4.0mm, Lead Pitch 0.4mm)



TYPICAL APPLICATION



Notes: The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

OVERVIEW

KA44370A is a gate driver IC for driving single-phase motors.

The output stage, which can directly drive an external power MOSFET at 48V, is mounted in a small 4mm x 4mm QFN package, making it possible to mount the IC on a small motor despite the 48V requirement.

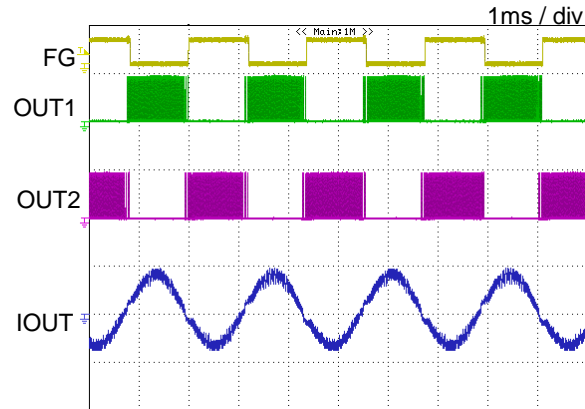
Speed commands can be input via PWM input or DC voltage, and speed feedback control is also supported.

The motor drive current can be selected from a sinusoidal wave for low vibration and a trapezoidal wave for high-speed rotation. It also supports adjustment of the advanced phase to achieve high-speed rotation, providing optimal motor drive control for a variety of applications.

APPLICATIONS

Single-phase Fan Motors for Server, Cellular Base station, Industry, and Home appliance

TYPICAL CHARACTERISTICS



Condition:

- $V_{CC} = 48V$, $C_{VM} = 10\mu F$, $C_{VCC} = 0.1\mu F$, $R_{CS} = 0.22\Omega$,
- $V_{VSP} = \text{PWM input mode (30kHz, Duty30\%)}$,
- $V_{TMAX} = 0.3V$, Motor current wave = sinusoidal wave

Contents

IMPORTANT NOTICE2

FEATURES.....3

OVERVIEW.....3

TYPICAL APPLICATION3

1. ELECTRICAL CHARACTERISTICS5

 1.1 Absolute Maximum Ratings.....5

 1.2 Power Dissipation Rating6

 1.3 Recommended Operating Conditions7

 1.4 Electrical Characteristics8

2. PIN DESCRIPTION11

 2.1 Pin Configuration11

 2.2 Pin Functions12

3. BLOCK DIAGRAM.....14

4. OPERATION.....15

 4.1 Control Mode Table15

 4.2 VCC Start-up and Stop Operating16

 4.3 Start-up Mode / Normal Mode Switching.....17

 4.4 FG(Frequency Generator) / LD(Lock Detect) terminal Output Signal Selection17

 4.5 Relationship between Hall Input, FG Output, and Motor Output.....18

 4.6 Motor Lock Protection20

 4.7 Standby Power Consumption Reduction Mode Selection.....22

 4.8 VSP Terminal Input Mode Selection23

 4.9 Output PWM Control Setting24

 4.10 VSP Speed Control Method26

 4.11 Motor Current Control.....27

 4.12 Motor Current Waveform30

 4.13 Motor Current Advanced Phase Control32

 4.14 Slow Acceleration / Deceleration Time.....33

 4.15 Speed Command Input / Output Polarity and Gain Adjustment.....35

 4.16 Register List.....37

 4.17 OTP Control Interface Specification40

 4.18 OTP Control Mode List.....41

 4.19 OTP Write Inspection Flow.....50

 4.20 OTP Program Environment and Precautions for Using OTP51

 4.21 Protection Function.....52

5. PACKAGE INFORMATION53

 5.1 Outline Drawing53

USAGE NOTES.....54

REVISION HISTORY.....56

IMPORTANT NOTICE.....57

1. ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	V_{CC}	-0.3 ~ +100	V	*1
Operating Ambient Temperature	T_{OPR}	-40 ~ +105	°C	*2
Junction Temperature	T_j	-40 ~ +150	°C	*2
Storage Temperature	T_{STG}	-55 ~ +150	°C	*2
Input Voltage Range	$V_{HP}, V_{HN}, V_{PROG}, V_{SDI}, V_{SCK}, V_{VSP}, V_{LVD_H}$	-0.3 ~ +6	V	—
	V_{CS}	$V_{50} + 0.3$	V	—
	V_{CSGND}	-0.3 ~ +0.3	V	—
Input Current Range	I_{VSP}	-1 ~ +1	mA	—
Output Voltage Range	$V_{FG/LD}$	+40	V	—
	V_{VB1}, V_{VB2}	+100	V	*3
	V_{OUT1P}, V_{OUT2P}	+100	V	*3
	V_{OUT1N}, V_{OUT2N}	+13	V	*3
	V_{50}, V_{HB}	-0.3 ~ +6	V	*3
	V_{CLAMP}	+100	V	*3
Output Current Range	$I_{OUT1P}, I_{OUT1N}, I_{OUT2P}, I_{OUT2N}$	-100 ~ +100	mA	*4,*5
	$I_{FG/LD}$	+10	mA	—
	I_{HB}	-3 ~ 0	mA	*4,*5
	I_{V50}	-10 ~ 0	mA	*4,*5
	I_{CLAMP}	5	mA	*4,*5
Allowable Potential Difference between Pins	$V_{OUT1P} - V_{OUT1}, V_{OUT2P} - V_{OUT2}$	+12	V	*3
ESD	HBM	2	kV	—

Notes: This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

- *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
- *2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for $T_a = 25^\circ\text{C}$.
- *3: Applying external voltage into these pins is prohibited. Do not exceed the stated ratings even in transient state.
- *4: Applying external current into these pins is prohibited. Do not exceed the stated ratings even in transient state.
- *5: Ensure no issue arisen due to temperature increase in IC.

1.2 Power Dissipation Rating

Package	θ_{j-a}	PD (Ta=25 °C)	PD (Ta=105 °C)
QFN 32pin (4x4mm, Lead Pitch 0.4mm)	78.5 °C / W	1.59 W	0.57 W

Notes: For the actual usage, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

*1: Glass-Epoxy Substrate (2 Layers) [50 x 50 x 0.8 t](mm),
Heat dissipation fin: Die-pad, Soldered. (Heat dissipation via 2 layer board)

CAUTION



Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

1.3 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage Range	V_{CC}	8	—	76	V	*1
Input Voltage Range	V_{HP}, V_{HN}	0	—	1.5	V	*2
	V_{VSP}	0	—	V50	V	*2
External Constants	C_{VM}	—	10	—	μF	*3
	C_{VCC}	—	0.1	—	μF	*3
	C_{VB1}, C_{VB2}	—	0.047	—	μF	*3
	C_{V50}	—	0.1	—	μF	*3
Exposed Die Pad Voltage	V_{DAP}	—	0	—	V	—

- Notes
- *1: It is a value under the conditions which do not exceed the absolute maximum rating and the power dissipation.
 - *2: For setting range of input control voltage, refer to Electrical Characteristics and Operation.
 - *3: This value is an example. Operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.

1.4 Electrical Characteristics

V_{CC} = 48 V,

Note: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min.	Typ.	Max.		
Circuit Current							
Active VCC circuit current	I _{CC}	V _{CC} = 48 V	—	3.0	7.0	mA	—
Sleep VCC circuit current	I _{CCSL}	V _{CC} = 48 V	—	0.2	0.5	mA	—
Regulator Block							
Output voltage	V ₅₀	—	4.75	5.0	5.25	V	—
Output impedance	Z _{V50}	I _{V50} = - 5 mA	—	—	10	Ω	—
FG / LD Block							
Low-level output voltage	V _{FG/LD}	I _{FG/LD} = 5 mA	—	0.1	0.3	V	—
Output leak current	I _{LFG}	V _{FG/LD} = 40 V	—	—	5	μA	—
Hall Block							
Input dynamic range	V _{DHALL}	—	0	—	1.5	V	—
Pin input current	I _{HALL}	—	-1	0	1	μA	—
Hysteresis level Low to High	V _{Hhys1}	—	1	7.5	14	mV	—
Hysteresis level High to Low	V _{Hhys2}	—	-14	-7.5	-1	mV	—
Hysteresis width	V _{HHYS}	—	7.5	15	23	mV	—
HB Block							
Output voltage	V _{HB}	I _{HB} = 0 mA	2.3	2.7	3.1	V	—
Output impedance	Z _{HB}	I _{HB} = - 1 mA	—	270	300	Ω	—
VSP Speed Control Block (DC input mode, 8bit ADC input)							
Pin inflow current	I _{VSP}	—	-1	0	1	μA	—
Stop control input voltage (DC input mode)	V _{VSPMIN}	—	V ₅₀ * 0.18	V ₅₀ * 0.22	V ₅₀ * 0.26	V	—
Maximum speed input voltage (DC input mode)	V _{VSPMAX}	—	V ₅₀ * 0.55	V ₅₀ * 0.60	V ₅₀ * 0.65	V	—
VSP Speed Control Block (PWM input mode)							
Pin inflow current	I _{PWML}	—	-1	0	1	μA	—
Low-level input voltage (PWM input mode)	V _{PWML}	—	—	—	1	V	—
High-level input voltage (PWM input mode)	V _{PWMH}	—	2.4	—	—	V	—
Input frequency range (PWM input mode)	F _{PWM}	—	1	—	60	kHz	—
External MOSFET Gate Drive Output							
High-side MOSFET gate drive "High" output voltage 1	V _{OUTPH1}	I _{OUT*P} = 0 mA	7	9	11	V	—
High-side MOSFET gate drive "High" output voltage 2	V _{OUTPH2}	I _{OUT*P} = -100 mA, V _{VB*} = 9 V	4	—	—	V	—

1.4 Electrical Characteristics(continued)

V_{CC} = 48 V,

Note: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min.	Typ.	Max.		
High-side MOSFET gate drive "Low" output voltage 1	V _{OUTPL1}	I _{OUT*P} = 0 mA V _{OUT*} = 0 V, V _{OUT*P} - V _{OUT*} differential voltage	-0.1	0	0.1	V	—
High-side MOSFET gate drive "Low" output voltage 2	V _{OUTPL2}	I _{OUT*P} = 100 mA, V _{OUT*} = 0 V, V _{OUT*P} - V _{OUT*} differential voltage	—	—	1.5	V	—
V _B current when High-side MOSFET gate drive output is "High"	I _{VB}	I _{OUT*P} = 0 mA, V _{VB*} = 48 V	50	140	250	μA	—
Low-side MOSFET gate drive "High" output voltage 1	V _{OUTNH1}	I _{OUT*N} = 0 mA	9.5	10.9	12.5	V	—
Low-side MOSFET gate drive "High" output voltage 2	V _{OUTNH2}	I _{OUT*N} = -100 mA	5.5	8	—	V	—
Low-side MOSFET gate drive "Low" output voltage 1	V _{OUTNL1}	I _{OUT*N} = 0 mA	-0.1	0	0.1	V	—
Low-side MOSFET gate drive "Low" output voltage 2	V _{OUTNL2}	I _{OUT*N} = 100 mA	—	—	1.5	V	—
VCC Undervoltage Lock Out							
LVD_H Low-level input voltage	V _{LVDL}	—	—	—	V50 *0.2	V	—
LVD_H High-level input voltage	V _{LVDH}	—	V50 *0.8	—	—	V	—
Protection operating voltage at VCC rising 1	V _{LVD1R}	V _{LVD_H} = GND	—	6.7	—	V	—
Protection operating voltage at VCC falling 1	V _{LVD1F}	V _{LVD_H} = GND	5.7	6.2	6.7	V	—
Hysteresis width 1	V _{LVD1HYS}	V _{LVD_H} = GND	0.4	0.5	0.6	V	—
Protection operating voltage at VCC rising 2	V _{LVD2R}	V _{LVD_H} = V50	—	20	—	V	—
Protection operating voltage at VCC falling 2	V _{LVD2F}	V _{LVD_H} = V50	16	18	20	V	—
Hysteresis width 2	V _{LVD2HYS}	V _{LVD_H} = V50	1.5	2	2.5	V	—
Input pull-down resistor	R _{LVD_H}		—	400	—	kΩ	—
Motor Current Limiter							
Detection voltage 1	V _{CS1}	V _{CSGND} =0V	0.285	0.30	0.315	V	—
Detection voltage 2	V _{CS2}	V _{CSGND} =0V	0.238	0.25	0.262	V	*1
Detection voltage 3	V _{CS3}	V _{CSGND} =0V	0.19	0.20	0.21	V	*1
Detection voltage 4	V _{CS4}	V _{CSGND} =0V	0.14	0.15	0.16	V	*1
Clamp Voltage (VCC overvoltage protection)							
Internal voltage	V _{CLP}	I _{CLAMP} = 3 mA, V _{OUT*} = 0 V, V _{CLAMP} - V _{OUT*P} differential voltage	7.5	8.8	10.1	V	*1

Notes:

*1: Design reference value not tested during final production inspection.

1.4 Electrical Characteristics(continued)

V_{CC} = 48 V,

Note: T_a = 25°C±2°C unless otherwise noted.

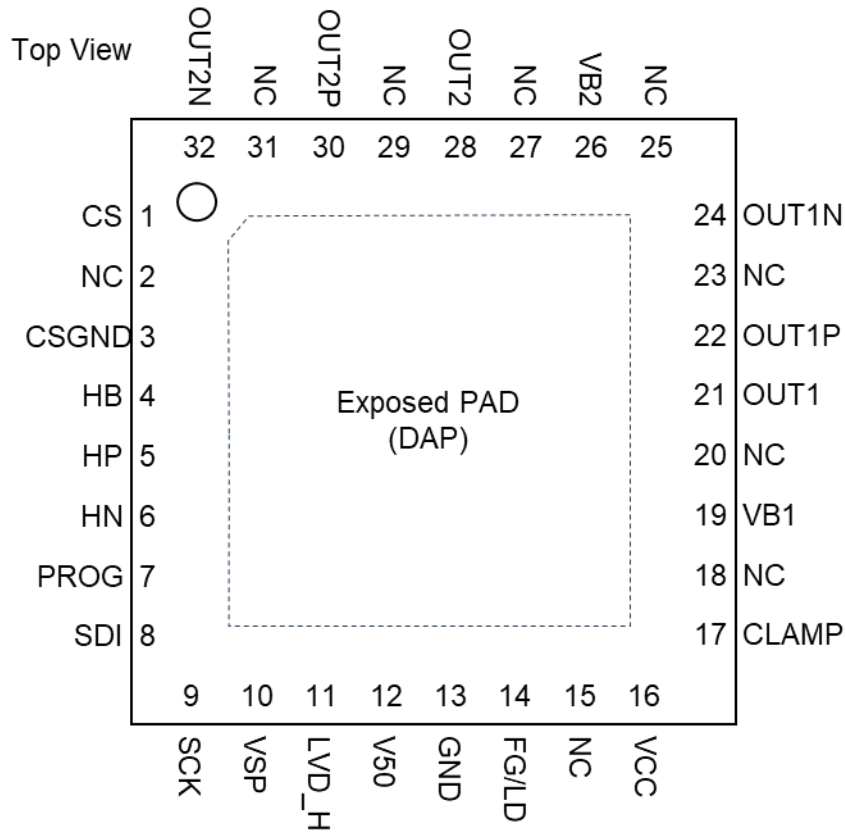
Parameter	Symbol	Condition	Limits			Unit	Note
			Min.	Typ.	Max.		
System Clock Block							
Clock frequency	f _{CLK}	—	23.75	25	26.25	MHz	—
OTP Setting Block (PROG / SDI / SCK)							
Low-level input voltage	V _{SETL}	Serial setting	—	—	1.0	V	—
High-level input voltage	V _{SETH}	Serial setting	2.4	—	—	V	—
Input pull-down resistor	R _{PROGIN}	—	—	20	—	kΩ	—
Thermal Protection							
Protection operating temperature	TSD _{ON}	—	—	160	—	°C	*2
Hysteresis width	TSD _{HYS}	—	—	25	—	°C	*2

Notes:

*2: Typical design value.

2. PIN DESCRIPTION

2.1 Pin Configuration



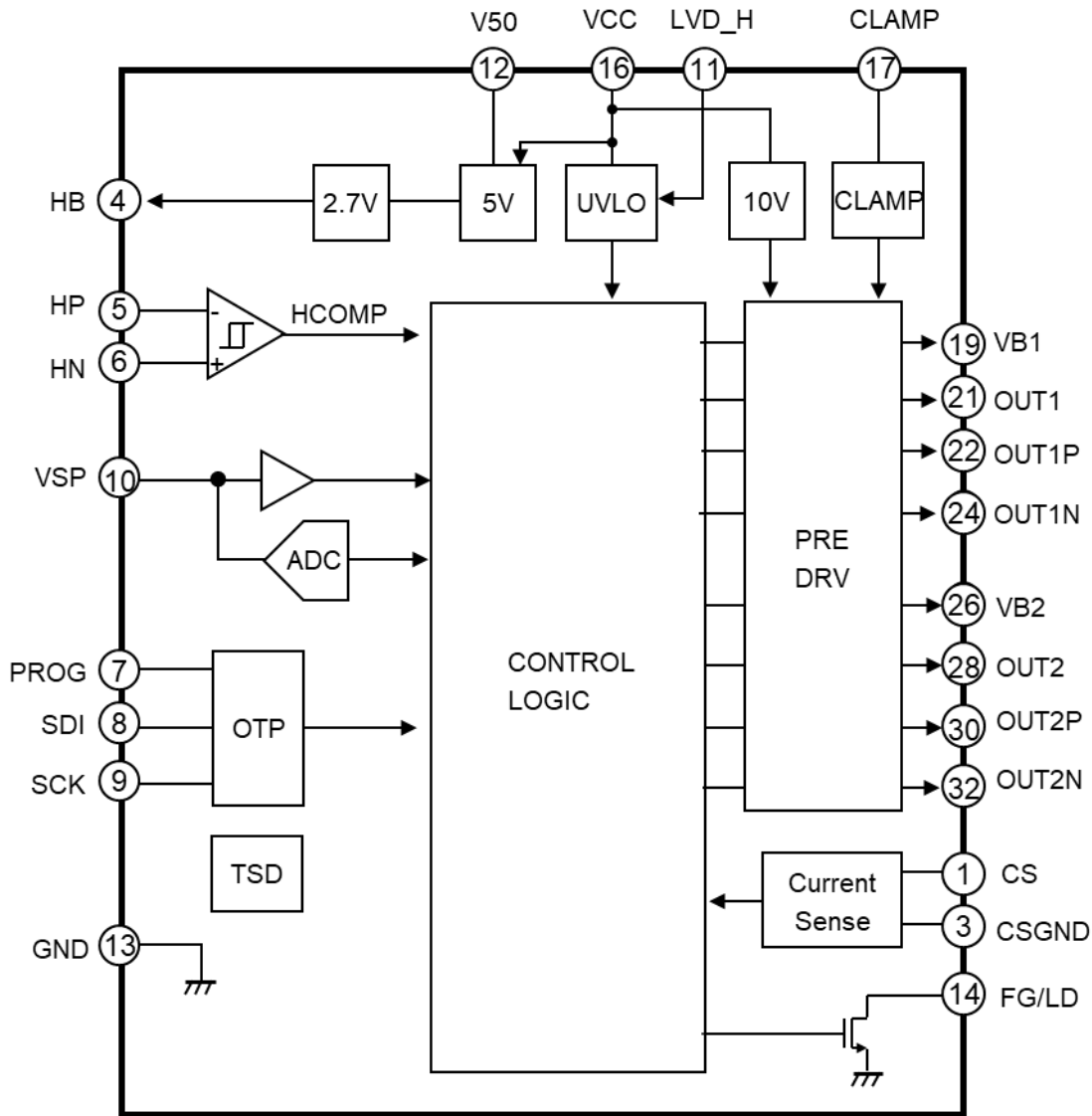
2.2 Pin Functions

Pin No.	Pin name	Type	Description
1	CS	Input	Motor current detection input (+)
2	NC	—	No Connection
3	CSGND	Input	Motor current detection input (-)
4	HB	Output	Hall element bias output
5	HP	Input	Hall amplifier input (+)
6	HN	Input	Hall amplifier input (-)
7	PROG	Input	Serial setting ENABLE input
8	SDI	Input	Serial setting DATA input
9	SCK	Input	Serial setting CLOCK input
10	VSP	Input	Motor speed control input (PWM / DC)
11	LVD_H	Input	VCC undervoltage lock out threshold voltage setting input
12	V50	Output	5V Internal reference voltage output
13	GND	Ground	Ground
14	FG / LD	Output	FG or LD output Serial setting READ output
15	NC	—	No Connection
16	VCC	Power	Power supply voltage input
17	CLAMP	Input	Zener diode connection for VCC clamp voltage setting
18	NC	—	No Connection
19	VB1	Output	OUT1 bootstrap voltage output
20	NC	—	No Connection
21	OUT1	Output	OUT1 output
22	OUT1P	Output	OUT1 High-side MOSFET gate drive output
23	NC	—	No Connection
24	OUT1N	Output	OUT1 Low-side MOSFET gate drive output
25	NC	—	No Connection
26	VB2	Output	OUT2 bootstrap voltage output
27	NC	—	No Connection
28	OUT2	Output	OUT2 output

2.2 Pin Functions (continued)

Pin No.	Pin name	Type	Description
29	NC	—	No Connection
30	OUT2P	Output	OUT2 High-side MOSFET gate drive output
31	NC	—	No Connection
32	OUT2N	Output	OUT2 Low-side MOSFET gate drive output
—	DAP	—	Exposed die pad

3. BLOCK DIAGRAM



Notes: This block diagram is for explanation purpose.
Part of the block diagram may be omitted, or it may be simplified.

4. OPERATION

Note) Typical values are shown unless otherwise noted.

Note) The recommended parameter settings are just examples. When designing a mass production set, please use it at your own risk after carrying out sufficient evaluation and verification.

4.1 Control Mode Table

•VCC undervoltage lock out (UVLO) threshold voltage

Pin No.	Pin name	Description	Setting Voltage		Remarks
			Low	High	
11	LVD_H	VCC undervoltage lock out threshold voltage setting	•VCC UVLO operation: 6.2V •VCC UVLO release: 6.7V	•VCC UVLO operation: 18V •VCC UVLO release: 20V	Connect to GND for Low setting, and to V50 for High setting with the board pattern.

•OTP write control

Pin No.	Pin name	Description	Setting Voltage		Remarks
			Low	High	
7	PROG	OTP write control	Normal operation	OTP can be set and motor stop	OTP control mode is entered by writing the password register setting to the SDI and SCK terminals while PROG="H".

4.2 VCC Start-up and Stop Operating

The motor starts operating at a maximum of 75ms after the VCC undervoltage protection detection function is released. The FG / LD terminal outputs "H" when VCC terminal is below the VCC undervoltage protection release threshold or when the V50 terminal is below 3.3V. When VCC terminal is above the VCC undervoltage protection release threshold and the V50 terminal is 3.3V or higher, FG will be output based on the Hall input polarity when FG is selected, and motor lock protection output will be output when LD output is selected. FG or LD output, FG / LD terminal will output "L" immediately after startup for motor lock protection release. If $V50 > 3.3V$ and FG is selected in the memory setting for the FG / LD output signal, the FG output reflects the Hall input polarity. On the other hand, if LD output is selected, it is "L" output that indicates lock protection release.

Immediately after the undervoltage protection is released, the FG / LD will output "L". Therefore, when selecting FG, the frequency immediately after motor start-up may differ from the actual frequency depending on the polarity of the Hall input.

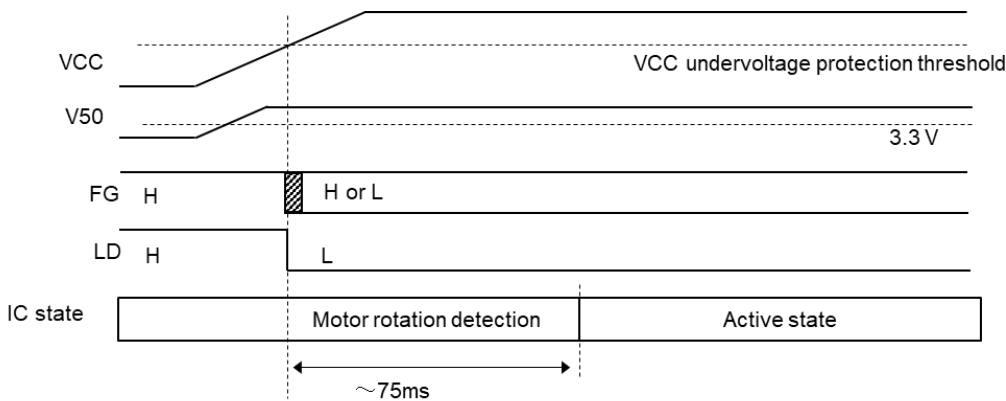


Fig. 4-1 Operation at start-up

When the VCC voltage drops below the VCC undervoltage protection threshold at power-down, the motor operation is stopped. FG / LD output goes "H" at $V50 < 3.2V$.

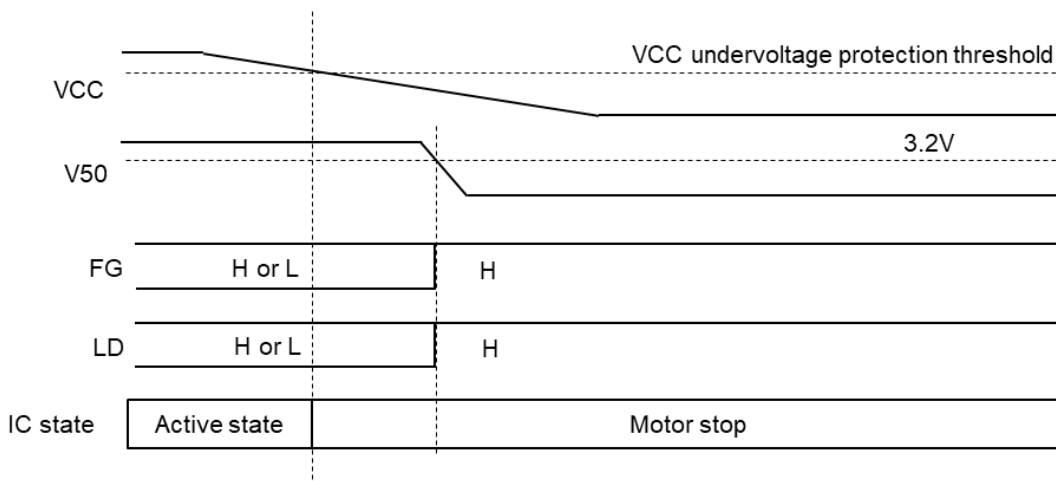


Fig. 4-2 Operation at stop

4.3 Start-up Mode / Normal Mode Switching

If the FG frequency is 6.67Hz or less (200rpm for a 4-pole motor), the motor will enter start-up mode regardless of the memory settings, and the motor output will be a square wave current waveform with the advanced phase of 0deg. Transition from start-up mode to normal mode occurs when FG frequency > 6.67Hz (200rpm for 4-pole motor). The motor output in normal mode will be the advanced phase value and motor current waveform set in the internal memory.

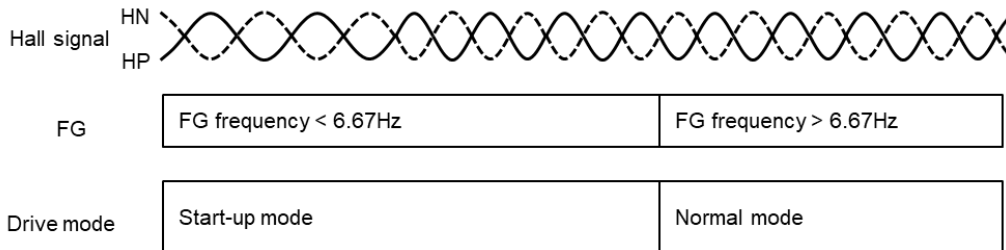


Fig. 4-3 Start-up mode / Normal mode switching

4.4 FG(Frequency Generator) / LD(Lock Detect) terminal Output Signal Selection

It is possible to select the output signal of FG / LD SW_{FG_LD} in the internal memory. Hall FG signal is output when FG is selected. On the other hand, when LD is selected, motor lock protection detection is output. Motor lock protection detection outputs "H" when protection is activated and "L" when protection is released. FG / LD is an open-drain output.

Address	Bit	Item	Variable	Default	Recommended	Description
0x27	D2	FG / LD terminal output signal selection	SW _{FG_LD}	1' b0	1' b0	1' b0: Rotation speed signal (FG) 1' b1: Motor lock protection detection signal (LD)

4.5 Relationship between Hall Input, FG Output, and Motor Output

•Hall Input and FG Output

Hall hysteresis comparator carries out motor rotor position detection. If the input amplitude of the Hall signal is small, efficiency may deteriorate during motor operation or noise issues may occur, so please ensure the Hall amplitude to be as large as possible. Recommendation is $HP-HN \geq 100mV_{pp}$. Also, if the hole chattering occurs, put capacitor C_{HALL} between HP and HN.

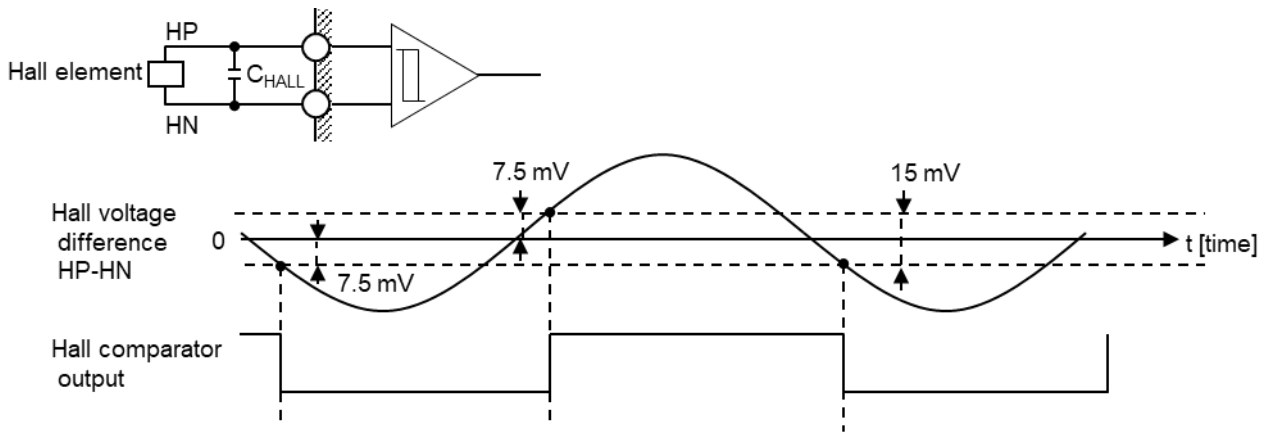


Fig. 4-4 Hall comparator threshold

The relationship between Hall voltage, FG, and motor output is shown in the figure below. It outputs one cycle of FG pulse one cycle for the one cycle sinusoidal wave of Hall, if FG is selected for the FG / LD output setting.

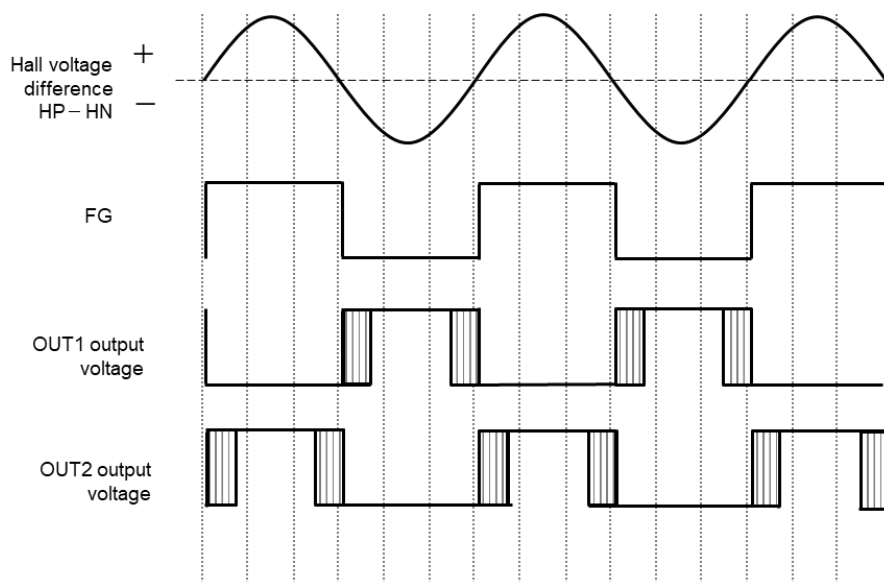


Fig. 4-5 Relationship between Hall input, FG output, and motor output

4.5 Relationship between Hall Input, FG Output, and Motor Output (continued)

•HB terminal and Hall signal

It is possible to bias the Hall element from HB terminal.

If the Hall element is biased directly from HB terminal, the IC may heat up, but adding a current limiting resistor R_{HB} to the connection path with the Hall element will help to suppress heat generation in the IC. However, the amplitude of the Hall signal will become proportionally smaller, so perform sufficient evaluation before setting the resistance value.

If heat generation is a concern, bias the Hall element with an NPN emitter follower or NMOS source follower with HB terminal as the control terminal.

In that case, adjust the resistor values of R_{HB_E} and R_{HB_S} so that the zero-cross voltage of the Hall signal is 1.5V or less. In addition, we recommend that the amplitude of the Hall signal be 100mVp-p or more.

Add capacitor C_{HB} as a noise suppression measure if necessary. Set the capacitor value from Open to 0.1 μ F.

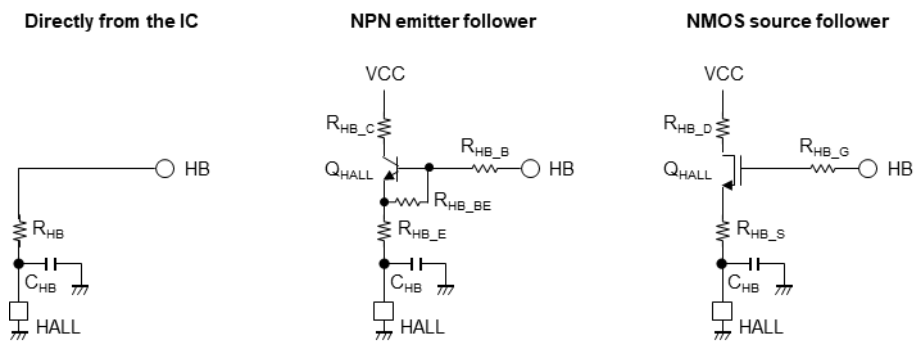


Fig. 4-6 Example of HB terminal peripheral circuit

Symbol	Min.	Typ.	Max.	Unit	Note
R_{HB_B}, R_{HB_G}	—	1	—	k Ω	*1
R_{HB_C}, R_{HB_D}	—	100	—	Ω	*1
R_{HB_BE}	—	10	—	k Ω	*1
C_{HB}	—	—	0.1	μ F	*1
C_{HALL}	—	—	0.01	μ F	*1

*1: This value is an example. Operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.

4.6 Motor Lock Protection

If the FG / LD output selection is FG, and no FG signal continues for longer than the lock protection operation time T_{LOCKON} set in the internal memory while the motor is operating, the motor output will turn OFF, and if the FG / LD output selection is LD, the output will switch from "L" to "H". If the motor lock protection state continues for the $T_{LOCKOFF}$ time set in the internal memory, the protection will be canceled when the falling edge of HP-HN occurs for 3 counts, and the FG / LD terminal output will switch from "H" to "L".

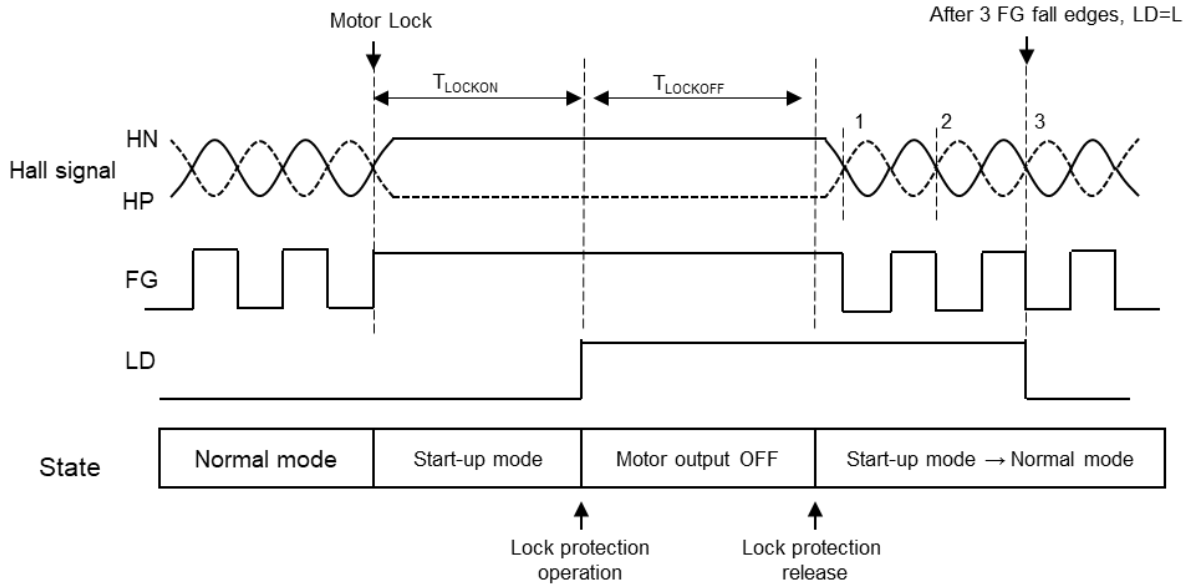


Fig. 4-7 Lock Protection Time for Detection and Release

This IC has a quick start function. The lock protection operation can be canceled by inputting a stop command (5ms or more) and re-inputting VSP. By re-inputting VSP, the motor stop state can be changed to the motor operating state without waiting for the lock protection release time $T_{LOCKOFF}$.

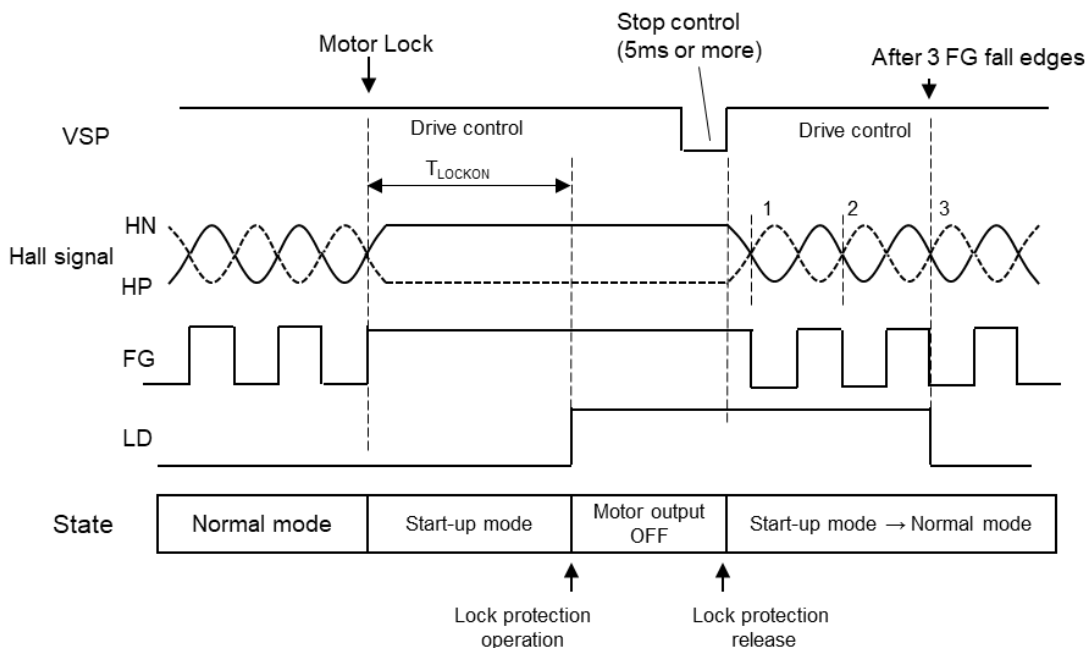


Fig. 4-8 Quick start when motor lock protection is in operation

4.6 Motor Lock Protection(continued)

Address	Bit	Item	Variable	Default	Recommended	Description
0x20	D7	Lock Protection Detection Time	T _{LOCKON}	3' b000	3' b000	3' b000: Lock protection invalid, 3' b001: 0.3s, 3' b010: 0.5s, 3' b011: 1.0s, 3' b100: 1.5s, 3' b101: 2.0s, 3' b110: 2.5s, 3' b111: 3.0s
	D6					
	D5					
0x21	D7	Lock Protection Release Time	T _{LOCKOFF}	1' b0	1' b0	1' b0: 5 times the lock protection detection time $T_{LOCKOFF} = T_{LOCKON} \times 5$ 1' b1: 10 times the lock protection detection time $T_{LOCKOFF} = T_{LOCKON} \times 10$

4.7 Standby Power Consumption Reduction Mode Selection

It is possible to enable or disable the standby power consumption reduction function using the internal memory. If it is enabled, when VSP's stop control and motor rotation speed < 200rpm (for a 4-pole motor) continues for lock protection operation time T_{LOCKON} , it switches to standby power consumption reduction mode (SLEEP mode) to reduce current consumption, and set HB="OFF", FG / LD output="H". Standby power consumption reduction mode can be canceled by inputting a start command via the VSP terminal.

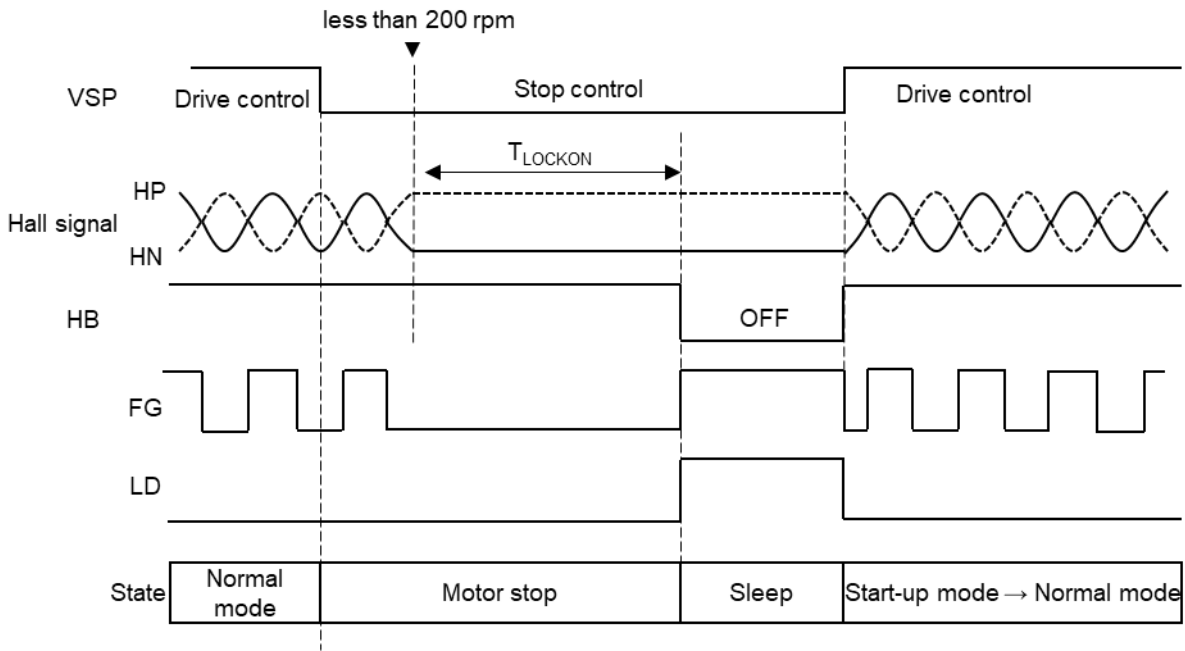


Fig. 4-9 SLEEP mode description

Address	Bit	Item	Variable	Default	Recommended	Description
0x27	D4	Standby Power Consumption Reduction Mode Selection	SW _{SLEEP}	1' b0	1' b0	1' b0: Standby power consumption reduction mode invalid 1' b1: Standby power consumption reduction mode valid

4.8 VSP Terminal Input Mode Selection

The internal memory allows selection of PWM input mode or DC input mode as the speed command signal input to the VSP terminal.

In DC input mode, you can set the speed command with a DC voltage (input D range 1.1V to 3.0V).

In PWM input mode, you can input a PWM signal with an input L level voltage of 0V, an input H level voltage of 5V, and a frequency range of 1 to 60kHz, and set the speed command with duty.

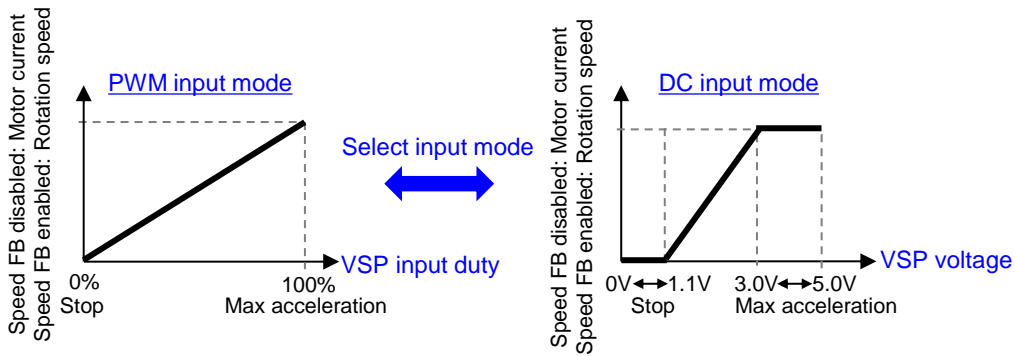


Fig. 4-10 PWM / DC input mode

Address	Bit	Item	Variable	Default	Recommended	Description
0x21	D0	VSP terminal Speed Command Input Signal Selection	VSP _{IN}	1' b0	1' b1	1' b0: DC input mode, 1' b1: PWM input mode

4.9 Output PWM Control Setting

•Synchronous Rectification Dead Time Adjustment

This IC uses synchronous rectification. Please set the synchronous rectification dead time T_{DED} to prevent penetration of High-side and Low-side MOSFETs after confirming the setting according to the MOSFET used, the gate resistance, and the gate-source (GS) capacitance. Synchronous rectification can be expected to reduce MOSFET heat generation, reduce noise, and reduce vibration.

•PWM ON Mask Time Adjustment

This IC monitors the voltage generated between CS and CSGND every PWM cycle to control the motor current. Please check the PWM noise generated when PWM is on and set the PWM ON mask time T_{ON} . If the PWM ON mask time is set too short, PWM noise may be falsely detected, causing the motor current waveform to become unstable. If the PWM ON mask time is set too long, it may cause distortion of the motor current zero crossing waveform.

•Output PWM Frequency Selection

PWM frequency F_{PWM} can be selected between 20kHz and 30kHz.

•High-side MOSFET ON Duration Time Selection

This IC uses the bootstrap method to drive the high-side Nch MOSFET. If the high-side MOSFET is always on, the gate-source voltage of the high-side MOSFET will drop, so if the high-side MOSFET is kept on for the time set by the high-side MOSFET ON duration T_{BOOT} , the high-side MOSFET will be forcibly turned off and the bootstrap capacitance will be charged. If the bootstrap capacitance is large, the gate voltage of the high-side MOSFET may not rise when the motor starts. Also, if the bootstrap capacitance is small, the drop in the gate-source voltage when the high-side MOSFET gate drive output is high becomes significant, which may cause problems such as heat generation in the MOSFET.

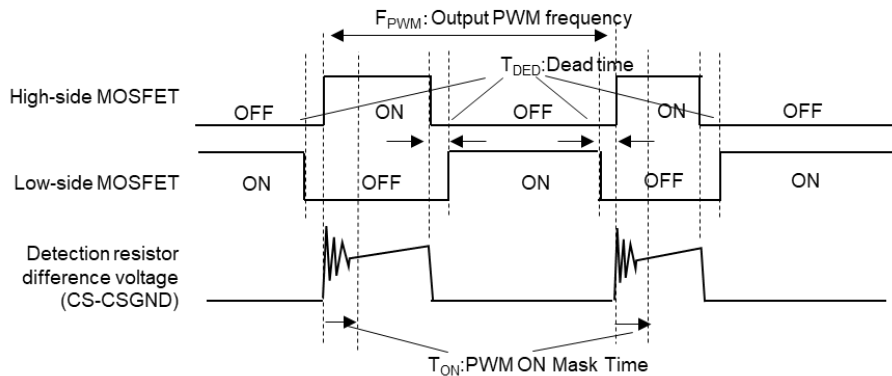


Fig. 4-11 Operation in PWM input mode

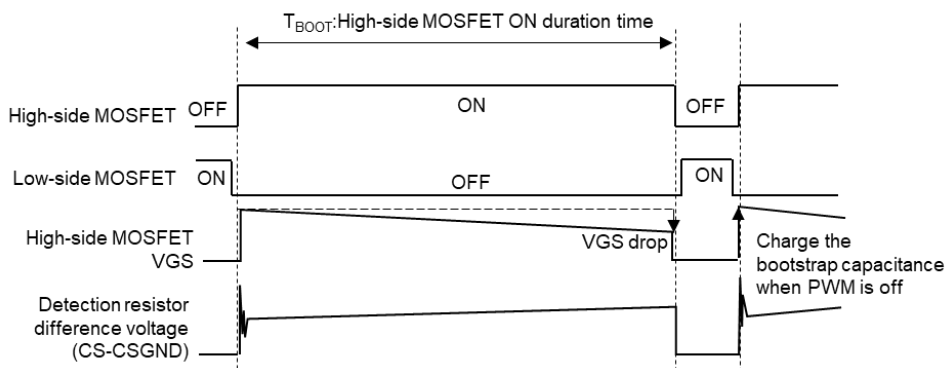


Fig. 4-12 High-side MOSFET ON duration time

4.9 Output PWM Control Setting(continued)

Address	Bit	Item	Variable	Default	Recommended	Description
0x21	D6	Synchronous Rectification Dead Time Adjustment	T_{DED}	2' b00	2' b10	2' b00: Non synchronous rectification, 2' b01: 1.0 μ s, 2' b10: 2.0 μ s, 2' b11: 3.0 μ s
	D5					
	D4	PWM ON Mask Time Adjustment	T_{ON}	2' b00	2' b01	2' b00: 1.0 μ s, 2' b01: 2.0 μ s, 2' b10: 3.0 μ s, 2' b11: 4.0 μ s
	D3					
	D2	Output PWM frequency Selection	F_{PWM}	1' b0	1' b1	1' b0: 20kHz, 1' b1: 30kHz
0x27	D3	High-side MOSFET ON Duration Time Selection	T_{BOOT}	1' b0	1' b1	1' b0: 50 μ s, 1' b1: 200 μ s

Note) Please note that the recommended value for "Output PWM control setting" differs depending on the MOSFET and gate constants.

4.10 VSP Speed Control Method

Speed feedback control is selectable for VSP terminal input.
 When speed feedback control is disabled, motor current is controlled according to the VSP terminal input.
 When speed feedback control is enabled, the motor rotation speed is controlled according to the VSP terminal input.
 The maximum rotation speed for speed feedback is set by N_{MAX1} , N_{MAX2} .

Address	Bit	Item	Variable	Default	Recommended	Description
0x26	D6	Maximum Rotation Speed Setting when Speed Feedback Control is Enabled	N_{MAX1}	7' b 0000000	7' b0000000	$N_{MAX1} = 7' \text{ b}0000000$ & $N_{MAX2} = 2' \text{ b}00$: Speed feedback control disabled, Others: Speed feedback control enabled
	D5					
	D4					
	D3					
	D2					
	D1					
0x27	D1	N_{MAX2}	2' b00	2' b00		
	D0					

When speed feedback control is enabled, the maximum rotation speed is set based on the following formula.

$$\text{Maximum rotation speed [rpm]}: (720 / \text{Pole}) \times (N_{MAX1} + 1) \times 2^{N_{MAX2}}$$

*Pole: Number of motor poles, N_{MAX1} , N_{MAX2} : Parameter setting (Calculate by converting to decimal)

(Example) If you set the speed feedback maximum rotation speed $N_{MAX1} = 7' \text{ b}0110111$, $N_{MAX2} = 2' \text{ b}00$, when converted to a decimal number, $N_{MAX1} = 55$, $N_{MAX2} = 0$, for a 4-pole motor,
 Maximum rotation speed = $(720 / 4) \times (55 + 1) \times 2^0 = 10,080\text{rpm}$.
 At this time, if you set the speed feedback minimum rotation speed $V_{TMIN} = 3' \text{ b}100$ (= 12.5%),
 controlled at minimum rotation speed = $10,080\text{rpm} \times 12.5\% = 1,260\text{rpm}$.

Speed feedback gains G_{STEP0} and G_{STEP1} can change the responsiveness of speed feedback control. Check the transient characteristics such as settling time and overshoot / undershoot during motor acceleration / deceleration and set the optimal speed feedback gain.

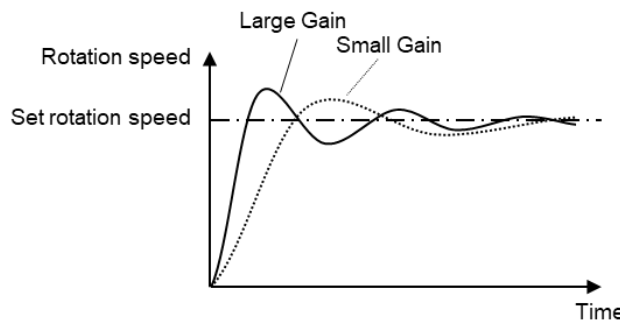


Fig 4-13 Response when speed feedback control is enabled

Note) If the speed feedback gain is too small, the starting torque may be insufficient, causing the lock protection to activate. Please perform sufficient evaluation and verification to ensure that the lock protection operation time is longer than the motor start-up time.

Address	Bit	Item	Variable	Default	Recommended	Description
0x26	D7	Responsiveness Adjustment when Speed Feedback Control is Enabled	G_{STEP1}	2' b00	2' b00	Adjust responsiveness with G_{STEP1} / G_{STEP0} . 2' b00: 1 (default), Largest gain 2' b01: 1/2, 2' b10: 1/4, 2' b11: 1/8 Smallest gain
0x27	D6		G_{STEP0}			

4.11 Motor Current Control

The maximum motor current adjustment $V_{T_{MAX}}$ sets the maximum value of the motor current. In combination with the current detection resistor R_{cs} , the maximum motor current I_{LIM} is limited by the following formula:

$$I_{LIM} = V_{T_{MAX}} / R_{cs}$$

Minimum rotation speed setting sets the minimum rotation speed with $V_{T_{MIN}}$.

Speed feedback control: Disabled

The minimum motor current I_{MIN} is set by the following formula, and the rotation speed is limited by the minimum current value

$$I_{MIN} = V_{T_{MAX}} \times V_{T_{MIN}} / R_{cs}$$

Speed feedback control: Enabled

The minimum RPM is set using the following formula

$$\text{Min. RPM} = \text{Max. RPM} \times V_{T_{MIN}}$$

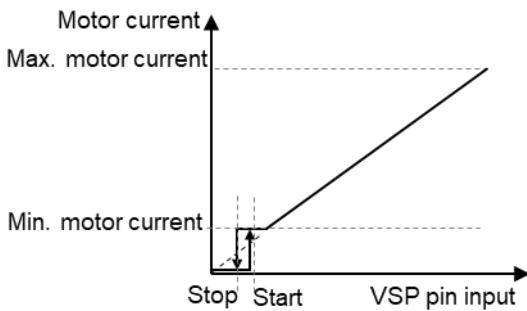


Fig. 4-14 speed feedback control: Disabled Maximum / Minimum Motor Current

The maximum / minimum motor currents set determines the maximum / minimum rotation speeds.

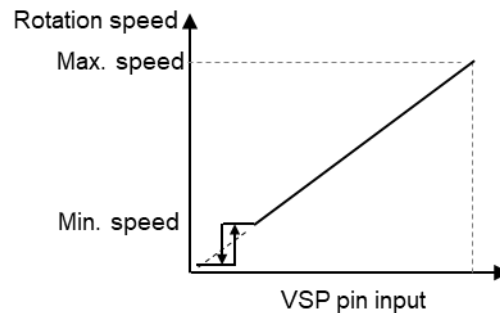


Fig. 4-15 speed feedback control: Enabled Maximum / Minimum rotation speed setting

The setting directly determines the maximum / minimum rotation speed

Address	Bit	Item	Variable	Default	Recommended	Description
0x20	D4	Minimum Rotation Speed Setting	$V_{T_{MIN}}$	3' b000	3' b000	When speed feedback control is disabled, the minimum motor current is controlled by the following formula. $I_{MIN} = V_{T_{MAX}} \times V_{T_{MIN}} / R_{cs}$
	D3					When speed feedback control is enabled, the minimum rotation speed is controlled by the following formula. $\text{Min. RPM} = \text{Max. RPM} \times V_{T_{MIN}}$
	D2					Please refer to the following table 4.11-1 for details
	D1	Maximum Motor Current Adjustment	$V_{T_{MAX}}$	2' b00	2' b10	2' b00: 0.30V, 2' b01: 0.25V, 2' b10: 0.20V, 2' b11: 0.15V
D0						

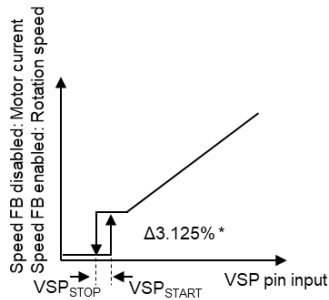
4.11 Motor Current Control (continued)

Table 4.11-1 Minimum rotation speed setting

No	VT _{MIN}			Speed feedback control disabled Minimum motor current [A]	Speed feedback control enabled Minimum rotation speed [rpm]
	0x20 D4	0x20 D3	0x20 D2		
0	0	0	0	$V_{T_{MAX}} \times 0.0\% / R_{cs}$	Max. rotation speed $\times 0.0\%$
1	0	0	1	$V_{T_{MAX}} \times 3.1\% / R_{cs}$	Max. rotation speed $\times 3.1\%$
2	0	1	0	$V_{T_{MAX}} \times 6.3\% / R_{cs}$	Max. rotation speed $\times 6.3\%$
3	0	1	1	$V_{T_{MAX}} \times 9.4\% / R_{cs}$	Max. rotation speed $\times 9.4\%$
4	1	0	0	$V_{T_{MAX}} \times 12.5\% / R_{cs}$	Max. rotation speed $\times 12.5\%$
5	1	0	1	$V_{T_{MAX}} \times 15.6\% / R_{cs}$	Max. rotation speed $\times 15.6\%$
6	1	1	0	$V_{T_{MAX}} \times 18.8\% / R_{cs}$	Max. rotation speed $\times 18.8\%$
7	1	1	1	$V_{T_{MAX}} \times 21.9\% / R_{cs}$	Max. rotation speed $\times 21.9\%$

4.11 Motor Current Control(continued)

Motor start threshold setting VSP_{START} sets the VSP threshold that initiates motor startup. Motor stop / non-stop selection VSP_{STOP} sets whether motor drive is stopped by the VSP input. If stop enable is selected, the VSP threshold for stopping has a hysteresis width of 3.125% relative to the motor start threshold. If stop disable is selected, the minimum rotation speed changes depending on the minimum rotation speed setting VT_{MIN} setting.



*Define VSP input dynamic range as 100%

Fig 4-16 VSP at start and stop setting

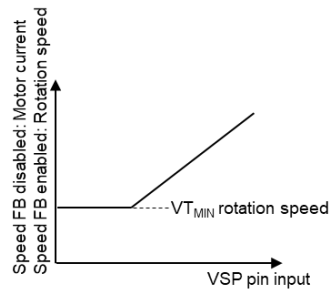


Fig 4-17 When not stop is selected in stop VSP setting

Address	Bit	Item	Variable	Default	Recommended	Description
0x22	D3	Motor stop Selection	VSP_{STOP}	1' b0	1' b0	1' b0: With stop Motor stop threshold = $VSP_{START} - 3.125\%$ VSP_{START} : Motor start threshold setting
	D2	Motor Start Threshold Setting	VSP_{START}	3' b000	3' b000	1' b1: Without stop
	D1					Motor start speed command input
	D0					0% - 21.9%, 3.125% step (8 divisions) Please refer to the following Table 4.11-2 for details.

Table.4.11-2 Start / Stop command threshold setting

No	VSP_{STOP}	VSP_{START}			PWM input mode $VSP_{IN} = 1' b1 \ *1$		DC input mode $VSP_{IN} = 1' b0 \ *1$	
	0x22 D3	0x22 D2	0x22 D1	0x22 D0	Start command threshold [%]	Stop command threshold [%]	Start command threshold [V]	Stop command threshold [V]
0	0	0	0	0	0.0	0.0	Do not set *2 (1.10)	Do not set *2 (1.10)
1	0	0	0	1	3.1	0.0	1.16	1.10
2	0	0	1	0	6.3	3.1	1.22	1.16
3	0	0	1	1	9.4	6.3	1.28	1.22
4	0	1	0	0	12.5	9.4	1.34	1.28
5	0	1	0	1	15.6	12.5	1.40	1.34
6	0	1	1	0	18.8	15.6	1.46	1.40
7	0	1	1	1	21.9	18.8	1.52	1.46
8	1	don't care			Without stop			

Note) The start/stop command threshold setting changes depending on VSP_{REV} , and the above setting value is the setting when $VSP_{REV} =$ positive gain is selected.

When $VSP_{REV} =$ negative gain is selected, it is set by the following formula.

$$VSP_{IN} = \text{PWM input mode: } 100\% - VSP_{START}$$

$$VSP_{IN} = \text{DC input mode: } (3.0V - 1.1V) \times (100\% - VSP_{START}) + 1.1V$$

*1: For information on setting VSP_{IN} , refer to chapter "4.8 VSP Terminal Input Mode Selection".

*2: This setting is prohibited because the motor may unintentionally start and stop repeatedly near the stop control voltage in DC input mode. If this setting is made, the settings in () will be used.

4.12 Motor Current Waveform

The motor current waveform can be set to a sinusoidal wave, trapezoidal wave, or current waveform control that changes from a sinusoidal wave to a trapezoidal wave. When using a sinusoidal wave that is advantageous for low noise and low vibration, set $VSP_{WAV0} = 4'b1111$ and $VSP_{WAV1} = \text{don't care}$.

When using a trapezoidal wave that is advantageous for high-speed rotation, set $VSP_{WAV0} = 4'b1111$, $VSP_{WAV1} = 4'b0000$. When using a current waveform that changes from sinusoidal wave to intermediate waveform and subsequently to trapezoidal wave, set it so that $VSP_{WAV0} < VSP_{WAV1}$. Speed feedback control: Set the medium wave start VSP and end VSP within the range so that the rotation speed changes smoothly with respect to the VSP input when disabled.

If you set $VSP_{WAV0} \geq VSP_{WAV1}$, there will be no intermediate waveform area, and the sinusoidal wave will be switched to the trapezoidal wave at the intermediate waveform start VSP VSP_{WAV0} . Please note that the rotational speed will fluctuate significantly at the switching point.

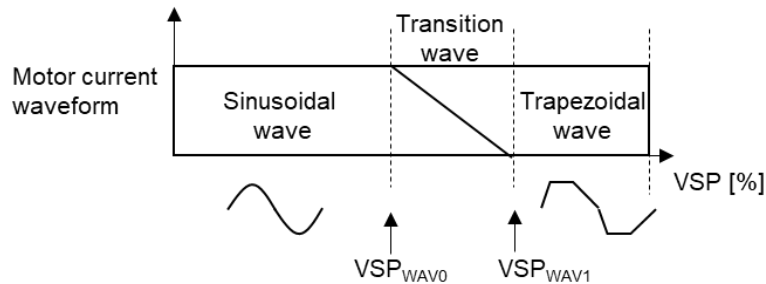


Fig. 4-18 Motor current waveform change with respect to VSP

Address	Bit	Item	Variable	Default	Recommended	Description
0x23	D7	Trapezoidal Wave Drive Start Threshold Setting	VSP_{WAV1}	4' b0000	4' b0000	Speed command input to start trapezoidal wave drive (transition wave drive completed) 0% - 93.8%, 6.25% step (16 divisions) 4' b0000: 0%, 4' b0001: 6.3%, 4' b0010: 12.5%, 4' b0011: 18.8%, 4' b0100: 25.0%, 4' b0101: 31.3%, 4' b0110: 37.5%, 4' b0111: 43.8%, 4' b1000: 50.0%, 4' b1001: 56.3%, 4' b1010: 62.5%, 4' b1011: 68.8%, 4' b1100: 75.0%, 4' b1101: 81.3%, 4' b1110: 87.5%, 4' b1111: 93.8%
	D6					
	D5					
	D4					
	D3	Sinusoidal Wave Drive Completion Threshold Setting	VSP_{WAV0}	4' b0000	4' b1111	
	D2					
	D1					
	D0					

Note) The setting value changes depending on the combination of the speed command input / output polarity selection VSP_{REV} and the VSP terminal speed command input signal selection VSP_{IN} . The above setting value is the setting when $VSP_{REV} = \text{positive gain}$, $VSP_{IN} = \text{PWM input mode}$ is selected.

For other combinations, the calculation formula for "trapezoidal wave drive start threshold setting VSP_{WAV1} " and "Sinusoidal wave drive completion threshold setting VSP_{WAV0} " is as follows.

VSP_{REV} / VSP_{IN}	
Negative gain / PWM input mode	$100\% - VSP_{WAV}^*$
Positive gain / DC input mode	$(3.0V - 1.1V) \times VSP_{WAV}^* + 1.1V$
Negative gain / DC input mode	$(3.0V - 1.1V) \times (100\% - VSP_{WAV}^*) + 1.1V$

Note) When speed feedback control is enabled, please note that the output PWM Duty is controlled such that the rotation speed is linear with respect to the speed command input to the VSP terminal.

4.12 Motor Current Waveform(continued)

For trapezoidal waves, the slope of rising SL1 and falling SL2 of one waveform cycle (360 electrical degrees) can be set to 10deg / 30deg.

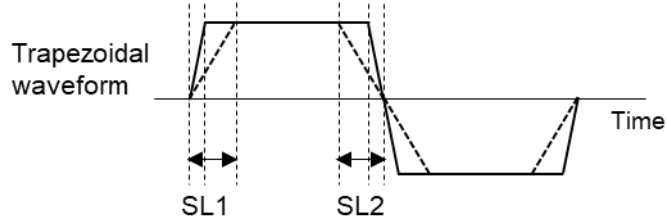


Fig. 4-19 Trapezoidal wave motor current rising / falling slope setting

Address	Bit	Item	Variable	Default	Recommended	Description
0x25	D7	Falling Slope Angle for Trapezoidal Wave	SL2	1' b0	1' b1	1' b0: 10deg 1' b1: 30deg
	D6	Rising Slope Angle for Trapezoidal Wave	SL1	1' b0	1' b0	1' b0: 10deg 1' b1: 30deg

4.13 Motor Current Advanced Phase Control

It is possible to set the advance phase control of the motor current. Settings can be made to suit the application, such as high efficiency and high-speed rotation.

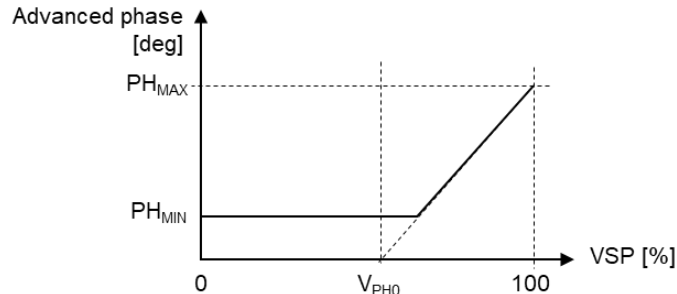


Fig. 4-20 Advanced phase setting

Address	Bit	Item	Variable	Default	Recommended	Description
0x24	D3	Motor Current Advanced Phase Start Threshold Setting	V _{PH0}	4' b0000	4' b0000	Speed command input at which motor current advanced phase start 0% - 93.8%, 6.25% step (16 divisions) 4' b0000: 0% 4' b0001: 6.3% 4' b0010: 12.5% 4' b0011: 18.8% 4' b0100: 25.0% 4' b0101: 31.3% 4' b0110: 37.5% 4' b0111: 43.8% 4' b1000: 50.0% 4' b1001: 56.3% 4' b1010: 62.5% 4' b1011: 68.8% 4' b1100: 75.0% 4' b1101: 81.3% 4' b1110: 87.5% 4' b1111: 93.8%
	D2					
	D1					
	D0					

Note) The above setting values are for when VSP_{REV} = positive gain and VSP_{IN} = PWM input mode are selected. For other combinations, the calculation formula for " Motor Current Advanced Phase Start Threshold Setting V_{PH0}" is as follows.

VSP _{REV}	/ VSP _{IN}	
Negative gain	/ PWM input mode	100% - V _{PH0}
Positive gain	/ DC input mode	(3.0V - 1.1V) × V _{PH0} + 1.1V
Negative gain	/ DC input mode	(3.0V - 1.1V) × (100% - V _{PH0}) + 1.1V

Note) When speed feedback control is enabled, please note that the output PWM Duty is controlled such that the rotation speed is linear with respect to the speed command input to the VSP terminal.

Address	Bit	Item	Variable	Default	Recommended	Description
0x25	D3	Maximum Motor Current Advanced Phase	PH _{MAX}	4' b0000	4' b0000	0deg - 42.2deg, 2.8125deg step (16 divisions) 4' b0000: 0deg 4' b0001: 2.8deg 4' b0010: 5.6deg 4' b0011: 8.4deg 4' b0100: 11.3deg 4' b0101: 14.1deg 4' b0110: 16.9deg 4' b0111: 19.7deg 4' b1000: 22.5deg 4' b1001: 25.3deg 4' b1010: 28.1deg 4' b1011: 30.9deg 4' b1100: 33.8deg 4' b1101: 36.6deg 4' b1110: 39.4deg 4' b1111: 42.2deg
	D2					
	D1					
	D0					
0x25	D5	Minimum Motor Current Advanced Phase	PH _{MIN}	2' b00	2' b00	0deg - 16.9deg, 5.625deg step (4 divisions) 2' b00: 0deg 2' b01: 5.6deg 2' b10: 11.3deg 2' b11: 16.9deg
	D4					

Note) When speed feedback control is enabled, please note that the output PWM Duty is controlled such that the rotation speed is linear with respect to the speed command input to the VSP terminal.

4.14 Slow Acceleration / Deceleration Time

Motor acceleration / deceleration time is controlled by the Slow Start Time T_{SLOW_R} and Slow Deceleration Time T_{SLOW_F} . The motor current is changed over the set time.

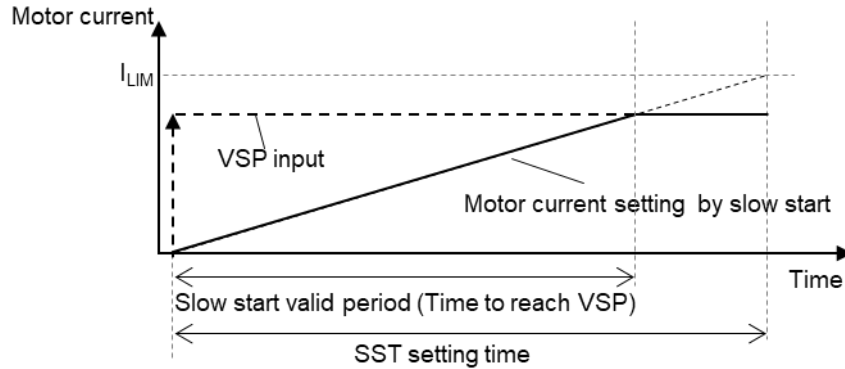


Fig. 4-21 Slow acceleration / deceleration

Address	Bit	Item	Variable	Default	Recommended	Description
0x22	D7	Slow Deceleration Time	T_{SLOW_F}	1' b0	1' b0	1' b0: 1x Slow Start Time $T_{SLOW_F} = T_{SLOW_R} \times 1$ 1' b1: 2x Slow Start Time $T_{SLOW_F} = T_{SLOW_R} \times 2$
0x22	D6	Slow Start Time (SST)	T_{SLOW_R}	3' b000	3' b000	Time to reach maximum motor current 0s - 11.2s, 1.6s step (8 divisions)
	D5					3' b000: 0s (SST invalid) 3' b001: 1.6s 3' b010: 3.2s 3' b011: 4.8s 3' b100: 6.4s 3' b101: 8.0s 3' b110: 9.6s 3' b111: 11.2s
	D4					

If acceleration or deceleration is performed during slow acceleration or slow deceleration, the operation will be as shown in Fig. 4-22.

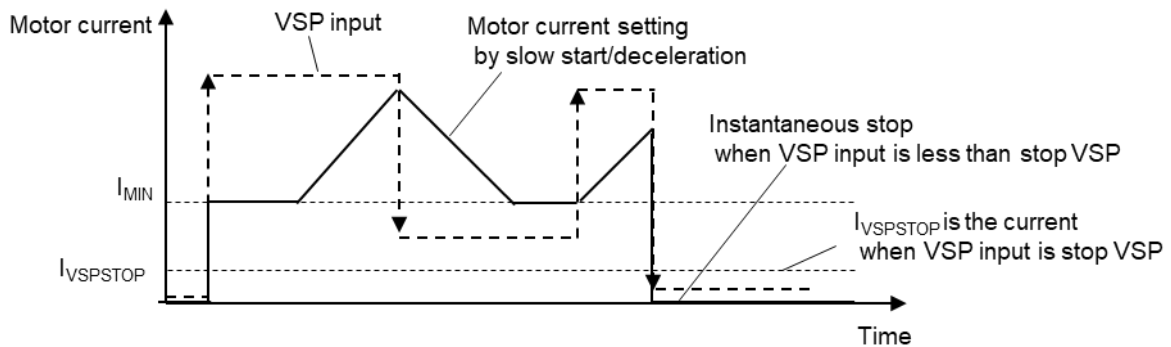


Fig. 4-22 Slow acceleration / deceleration during acceleration / deceleration

4.14 Slow Acceleration / Deceleration Time(continued)

Slow start at start-up

• Slow start when speed feedback control is disabled

When the motor starts from a stop state, it will start slowly according to the slow acceleration time T_{SLOW} setting. If a minimum rotation speed VT_{MIN} is set, the lower limit of the rotation speed will be limited by VT_{MIN} .

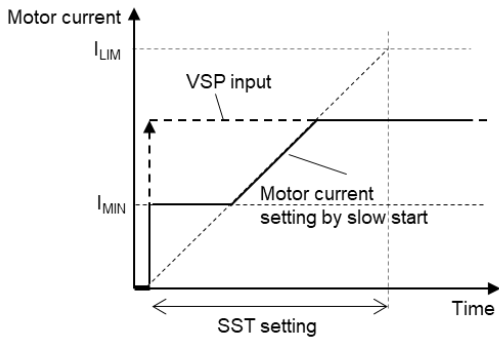


Fig. 4-23 $VSP > VT_{MIN}$

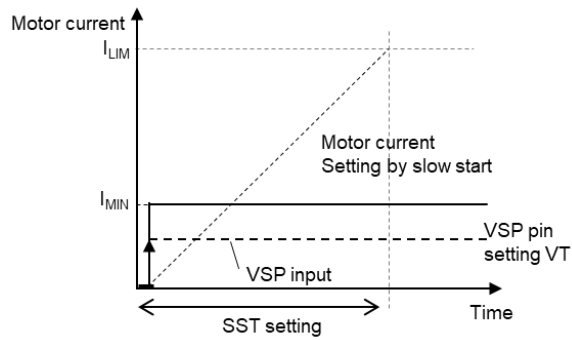


Fig.4-24 $VSP \leq VT_{MIN}$

• Slow start when speed feedback control is enabled

When the speed feedback control is enabled, the acceleration / deceleration time of the speed feedback control takes priority over either the settling time by the speed feedback or the slow acceleration / deceleration time, whichever is longer.

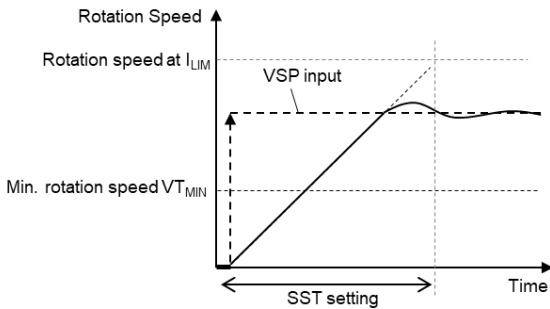


Fig. 4-25 acceleration / deceleration time \geq settling time

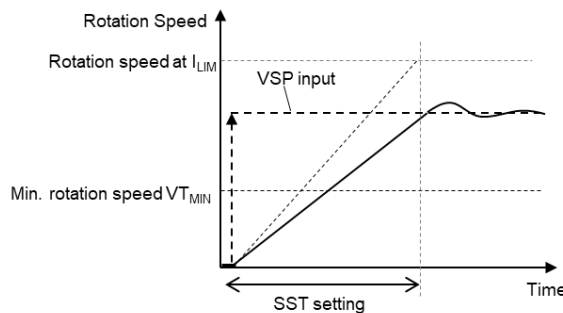


Fig.4-26 acceleration / deceleration time $<$ settling time

• About slow start during coasting

When starting during coasting, the slow acceleration / deceleration time is applied only when speed feedback control is enabled.

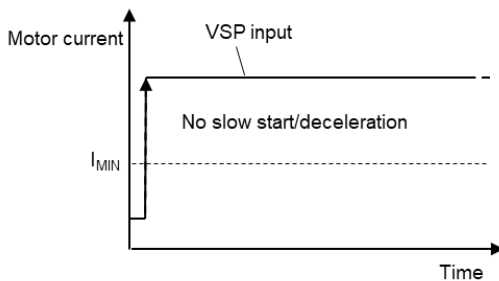


Fig. 4-27 With rotation at start-up, speed feedback control is disabled

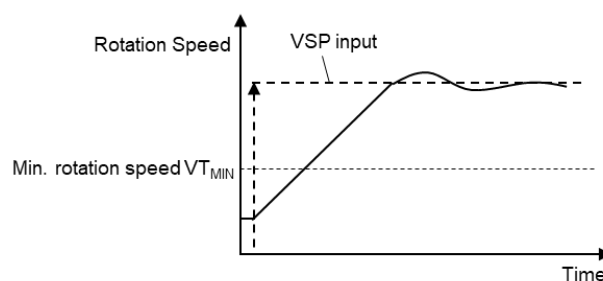


Fig.4-28 With rotation at start-up, speed feedback control is enabled

4.15 Speed Command Input / Output Polarity and Gain Adjustment

Speed Command Input / Output Gain Adjustment VSP_{MAX} sets the VSP input level for maximum output. The input / output gain polarity can be set using the VSP gain inversion mode VSP_{REV} .

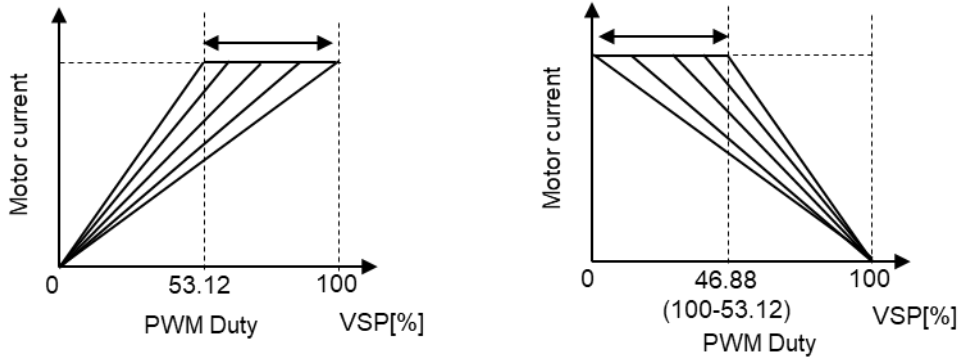


Fig. 4-29 VSP setting at $V_{T_{MAX}}$ in PWM input mode

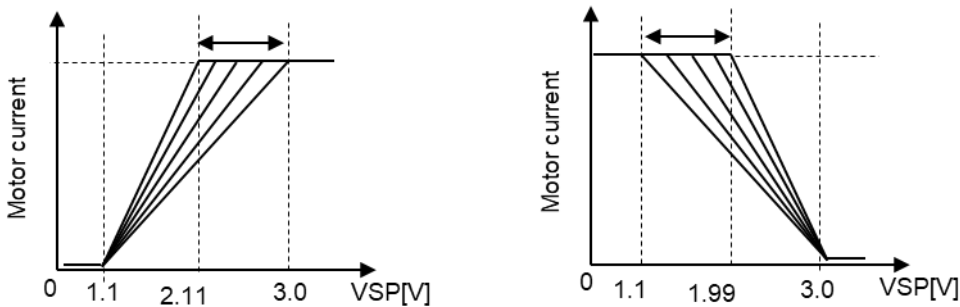


Fig. 4-30 VSP setting at $V_{T_{MAX}}$ in DC input mode

Address	Bit	Item	Variable	Default	Recommended	Description
0x21	D1	Speed Command Input / Output Polarity Selection	VSP_{REV}	1' b0	1' b0	1' b0: Positive gain 1' b1: Negative gain

Note) When negative gain is selected, the following parameter settings are also inverted. For details, see the chapters for each parameter.

- VSP_{MAX} : Speed command input for maximum motor current
- VSP_{START} : Speed command input for motor start-up
- VSP_{WAV1} : Speed command input for trapezoidal wave drive start
- VSP_{WAV0} : Speed command input for sinusoidal wave drive completion
- V_{PH0} : Speed command input for motor current advanced phase start

Address	Bit	Item	Variable	Default	Recommended	Description
0x24	D7	Speed Command Input / Output Gain Adjustment	VSP_{MAX}	4' b0000	4' b0000	Speed command input for maximum motor current 100% - 53.1%, 3.125% step (16 divisions) Please refer to the Table 4.15-1 for details.
	D6					
	D5					
	D4					

Note) The setting value changes depending on the combination of speed command input / output polarity selection VSP_{REV} and VSP terminal speed command input signal selection VSP_{IN} . The above setting value is the setting when VSP_{REV} = positive gain, VSP_{IN} = PWM input mode are selected. Please refer to Table 4.15-1 for setting values for other combinations.
Note) When speed feedback control is enabled, please note that the output PWM Duty is controlled so that the rotation speed is linear with respect to the speed command input to the VSP terminal.

4.15 Speed Command Input / Output Polarity and Gain Adjustment (continued)

Table 4.15-1 Speed command input for maximum motor

No	VSP _{REV}	VSP _{MAX}				Speed command input for maximum motor current [%]	
	0x21 D1	0x24 D7	0x24 D6	0x24 D5	0x24 D4	PWM input mode [%] VSP _{IN} = 1' b1 *1	DC input mode [V] VSP _{IN} = 1' b0 *1
0	0 (Positive gain)	0	0	0	0	100.0	3.00
1		0	0	0	1	96.9	2.94
2		0	0	1	0	93.8	2.88
3		0	0	1	1	90.6	2.82
4		0	1	0	0	87.5	2.76
5		0	1	0	1	84.4	2.70
6		0	1	1	0	81.3	2.64
7		0	1	1	1	78.1	2.58
8		1	0	0	0	75.0	2.53
9		1	0	0	1	71.9	2.47
10		1	0	1	0	68.8	2.41
11		1	0	1	1	65.6	2.35
12		1	1	0	0	62.5	2.29
13		1	1	0	1	59.4	2.23
14		1	1	1	0	56.3	2.17
15	1	1	1	1	53.1	2.11	
16	(Negative gain)	0	0	0	0	0.0	1.10
17		0	0	0	1	3.1	1.16
18		0	0	1	0	6.3	1.22
19		0	0	1	1	9.4	1.28
20		0	1	0	0	12.5	1.34
21		0	1	0	1	15.6	1.40
22		0	1	1	0	18.8	1.46
23		0	1	1	1	21.9	1.52
24		1	0	0	0	25.0	1.58
25		1	0	0	1	28.1	1.63
26		1	0	1	0	31.3	1.69
27		1	0	1	1	34.4	1.75
28		1	1	0	0	37.5	1.81
29		1	1	0	1	40.6	1.87
30		1	1	1	0	43.8	1.93
31		1	1	1	1	46.9	1.99

*1: For details about setting VSP_{IN}, refer to chapter "4.8 VSP Terminal Input Mode Selection".

4.16 Register List

Address	Bit	Item	Variable	Default	Recommended	Description	Page	
0x20	D7	Lock Protection Detection Time	T _{LOCKON}	3' b000	3' b000	3' b000: Lock protection invalid 3' b001: 0.3s 3' b011: 1.0s 3' b101: 2.0s 3' b111: 3.0s	20	
	D6							3' b010: 0.5s 3' b100: 1.5s 3' b110: 2.5s
	D5							
	D4	Minimum Rotation Speed Setting	V _{TMIN}	3' b000	3' b000	When speed feedback control is disabled, the minimum motor current is controlled by the following formula. When speed feedback control is enabled, the minimum rotation speed is controlled by the following formula.	27	
	D3							
	D2							
	D1	Maximum Motor Current Adjustment	V _{TMAX}	2' b00	2' b10	2' b00: 0.30V, 2' b10: 0.20V,	2' b01: 0.25V, 2' b11: 0.15V	27
D0								
0x21	D7	Lock Protection Release Time	T _{LOCKOFF}	1' b0	1' b0	1' b0: 5 times the lock protection detection time T _{LOCKOFF} = T _{LOCKON} × 5 1' b1: 10 times the lock protection detection time T _{LOCKOFF} = T _{LOCKON} × 10	20	
	D6	Synchronous Rectification Dead Time Adjustment	T _{DED}	2' b00	2' b10	2' b00: Non synchronous rectification, 2' b01: 1.0µs, 2' b10: 2.0µs, 2' b11: 3.0µs	24	
	D5							
	D4	PWM ON Mask Time Adjustment	T _{ON}	2' b00	2' b01	2' b00: 1.0µs, 2' b01: 2.0µs, 2' b10: 3.0µs, 2' b11: 4.0µs	24	
	D3							
	D2	Output PWM frequency selection	F _{PWM}	1' b0	1' b1	1' b0: 20kHz, 1' b1: 30kHz	24	
	D1	Speed Command Input / Output Polarity Selection	V _{SPREV}	1' b0	1' b0	1' b0: positive gain 1' b1: negative gain	35	
D0	VSP terminal Speed Command Input Signal Selection	V _{SPIN}	1' b0	1' b1	1' b0: DC input, 1' b1: PWM input	23		
0x22	D7	Slow Deceleration Time	T _{SLOW_F}	1' b0	1' b0	1' b0: 1x Slow Start Time T _{SLOW_F} = T _{SLOW_R} × 1 1' b1: 2x Slow Start Time T _{SLOW_F} = T _{SLOW_R} × 2	33	
	D6	Slow Start Time (SST)	T _{SLOW_R}	3' b000	3' b000	Time to reach maximum motor current 0s - 11.2s, 1.6s step (8 divisions)	33	
	D5							
	D4							
	D3	Motor Stop Selection	V _{SPSTOP}	1' b0	1' b0	1' b0: With stop Motor stop threshold = V _{SPSTART} – 3.125% 1' b1: Without stop	29	
	D2	Motor Start Threshold Setting	V _{SPSTART}	3' b000	3' b000	Motor start speed command input 0% - 21.9%, 3.125% step (8 divisions)	29	
	D1							
D0								

4.16 Register List (continued)

Address	Bit	Item	Variable	Default	Recommended	Description	Page
0x23	D7	Trapezoidal Wave Drive Start Threshold Setting	VSP _{WAV1}	4' b0000	4' b0000	Speed command input to start trapezoidal wave drive (transition wave drive completed) 0% - 93.8%, 6.25% step (16 divisions)	30
	D6						
	D5						
	D4						
	D3	Sinusoidal Wave Drive Completion Threshold Setting	VSP _{WAV0}	4' b0000	4' b1111	Speed command input for sinusoidal wave drive completed (transition wave drive start) 0% - 87.5%, 6.25% step (15 divisions), and 100%	30
	D2						
	D1						
	D0						
0x24	D7	Speed Command Input / Output Gain Adjustment	VSP _{MAX}	4' b0000	4' b0000	Speed command input for maximum motor current 100% - 53.1%, 3.125% step (16 divisions)	35
	D6						
	D5						
	D4						
	D3	Motor Current Advanced Phase Start Threshold Setting	V _{PH0}	4' b0000	4' b0000	Speed command input at which motor current advanced phase start 0% - 93.8%, 6.25% step (16 divisions)	32
	D2						
	D1						
	D0						
0x25	D7	Falling slope angle for trapezoidal wave	SL2	1' b0	1' b1	1' b0: 10deg, 1' b1: 30deg	31
	D6	Rising slope angle for trapezoidal wave	SL1	1' b0	1' b0	1' b0: 10deg, 1' b1: 30deg	31
	D5	Minimum Motor Current Advanced Phase	PH _{MIN}	2' b00	2' b00	0-16.9deg 5.625deg step (4 divisions)	32
	D4						
	D3	Maximum Motor Current Advanced Phase	PH _{MAX}	4' b0000	4' b0000	0-42.2deg 2.8125deg step (16 divisions)	32
	D2						
	D1						
	D0						

4.16 Register List (continued)

Address	Bit	Item	Variable	Default	Recommended	Description	Page
0x26	D7	Responsiveness Adjustment when Speed Feedback Control is Enabled 1	G _{STEP1}	2' b00	2' b00	Adjust responsiveness with G _{STEP1} G _{STEP0} . 2' b00: 1 (default), Largest gain 2' b01: 1/2, 2' b10: 1/4, 2' b11: 1/8 Smallest gain	26
	D6	Maximum Rotation Speed Setting when Speed Feedback Control is Enabled	N _{MAX1}	7' b 000000 0	7' b 0000000	N _{MAX1} = 7' b0000000 & N _{MAX2} = 2' b00 No speed control, Others Speed feedback control enabled	26
	D5						
	D4						
	D3						
	D2						
	D1						
	D0						
0x27	D7	PROTECT	PROTECT	1' b0	1' b1	Write data protection	—
	D6	Responsiveness Adjustment when Speed Feedback Control is Enabled 0	G _{STEP0}	2' b00	2' b00	Refer to Address: 0x26 D7	26
	D5	—	—	—	—	—	—
	D4	Standby Power Consumption Reduction Mode Selection	SW _{SLEEP}	1' b0	1' b0	1' b0: Standby power consumption reduction mode invalid 1' b1: Standby power consumption reduction mode valid	22
	D3	High-side MOSFET ON Duration Time Selection	T _{BOOT}	1' b0	1' b1	1' b0: 50µs, 1' b1: 200µs	24
	D2	FG / LD terminal output signal selection	SW _{FG_LD}	1' b0	1' b0	1' b0: Rotation speed signal (FG) 1' b1: Motor lock protection detection signal (LD)	17
	D1	Maximum Rotation Speed Setting when Speed Feedback Control is Enabled	N _{MAX2}	2' b00	2' b00	Refer to Address: 0x26 D0-6	26
D0							

4.17 OTP Control Interface Specification

Note) The following characteristics are design reference values, not guaranteed values.

This IC has internal memory (OTP: One Time Programmable read only memory) that allows you to set various functions. Please follow the timing constraints below when communicating.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency	F_{SCK}	—	—	—	500	kHz
Clock High period	T_{HI}	—	900	—	—	ns
Clock Low period	T_{LOW}	—	900	—	—	ns
PROG setup	T_{PRG_SET}	—	400	—	—	ns
PROG hold	T_{PRG_HD}	—	400	—	—	ns
PROG Low period	T_{PRG_LO}	—	4000	—	—	ns
SDI setup	T_{SDI_SET}	—	400	—	—	ns
SDI hold	T_{SDI_HD}	—	400	—	—	ns
FG / LD enable	T_{FG/LD_EN}	—	—	—	800	ns
FG / LD disable	T_{FG/LD_DIS}	—	—	—	800	ns

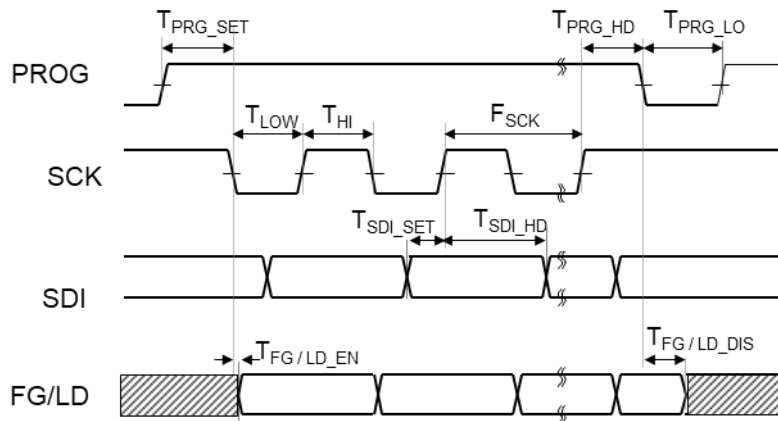


Fig. 4-31 OTP control timing constraints

4.18 OTP Control Mode List

OTP has the following five modes.

For parameter setting, use "OTP write mode", which writes data into the OTP, or "register setting mode", which does not write to the OTP. Use "register setting mode" for pre-verification before writing to the OTP.

To check data, use "OTP read mode" during inspection to make sure there is no prior writing, and after blowing the OTP in "OTP write mode", use "OTP margin check mode" to check all memory if each is blown and not blown.

Mode list

No.	Mode	Description	Page
1.	Register Setting Mode	You can set parameters without writing OTP. Use this mode for pre-verification. The values set in this mode will be initialized by VCC restart or entering standby power consumption reduction mode.	42
2.	Register Read Mode	You can read the register settings and the OTP write value when the register is not set after VCC restart.	43
3.	OTP Write Mode	Write to OTP. Writing to OTP retains parameter settings even after VCC is restarted. Writing to OTP is possible only once.	44
4.	OTP Read Mode	You can read the OTP write value.	46
5.	OTP Margin check Mode	Check the disconnection of OTP writing. OTP margin check 1 checks uncut OTP, and OTP margin check 2 checks disconnected OTP.	48

4.18 OTP Control Mode List (continued)

4.18.1 Register Setting Mode

In register setting mode, parameters can be set without writing OTP. Please use this mode to perform pre-verification before writing the OTP. Please note that the set parameters will be initialized when VCC is restarted or the IC enters standby power consumption reduction mode.

In register setting mode, the sequence is (1) Password input, (2) Parameter setting input.

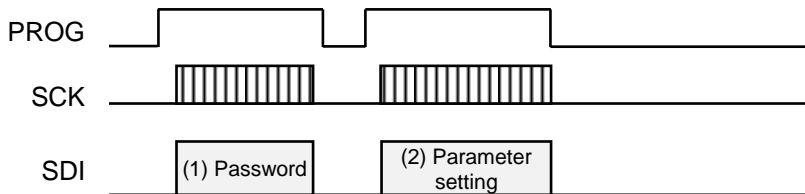


Fig.4-32 Register setting overall sequence

(1) Password input

Input password = "0xD6A3" with PROG = "H" state. After inputting the password, please set PROG = "L".

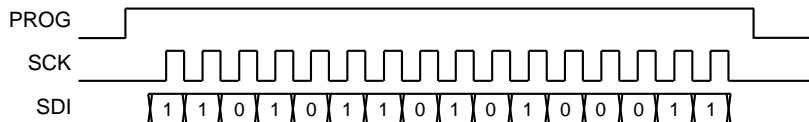


Fig.4-33 Register setting password input

(2) Parameter setting input

Switch PROG to "H", input the address for which you want to set the parameters (7 bits, A6~A0), the register access type to select write/read = "1' b0 (W)", and the data (8 bits, D7~D0), in that order. There is an automatic increment function to the next address, so when setting parameters to the next address, there is no need to input the next address. If you want to set parameters to an address other than the next address, input PROG = "L" and then input in the same procedure. After setting all parameters, set PROG = "L". This completes the register setting mode sequence.

To set parameters to an address other than the next address, input PROG = "L" and then follow the same procedure.

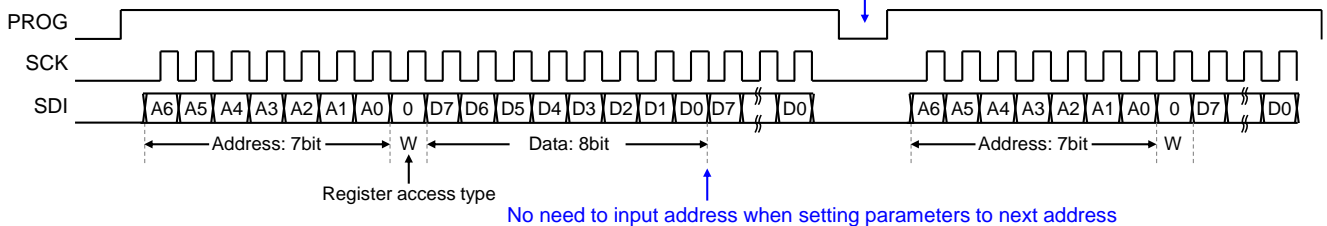


Fig.4-34 Register setting parameter setting command

4.18 OTP Control Mode List (continued)

4.18.2 Register Read Mode

In register read mode, parameters set in "1. Register Setting Mode", or the parameters written to the OTP in "3. OTP Write Mode" can be read if "1. Register Setting Mode" has not been executed after VCC startup. In register read mode, the sequence is (1) Password input, (2) Register read input.

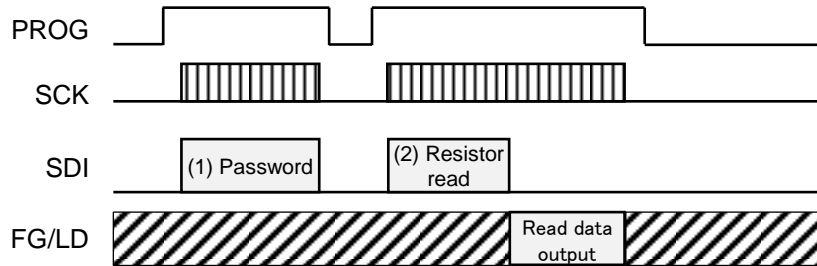


Fig. 4-35 Register read sequence

(1) Password input

Input password = "0xD6A3" with PROG = "H" state. After inputting the password, please set PROG = "L".

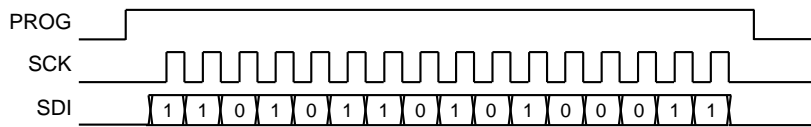


Fig. 4-36 Register read password input

(2) Register read

Switch PROG to "H", input the address for register read (7 bits, A6~A0) and register access type = "1" b1 (R), in that order, and data (8 bits, D7~D0) will be output from FG / LD. There is an automatic increment function for the next address, so there is no need to input the next address when reading a register at the next address. If you want to read a register other than the next address, input PROG = "L" and then follow the same procedure. After reading the register, set PROG = "L". This completes the register read mode sequence.

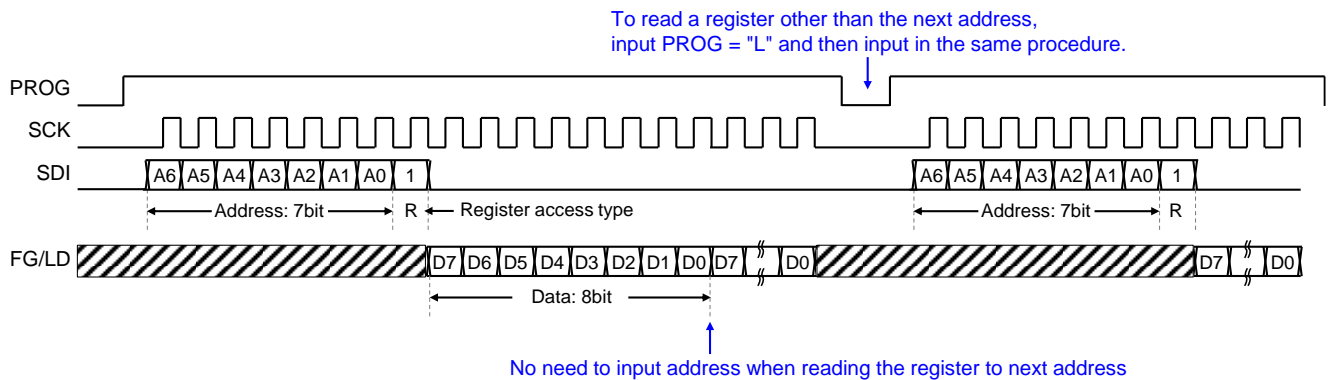


Fig. 4-37 Register read command

4.18 OTP Control Mode List (continued)

4.18.3 OTP Write Mode

Overview

In OTP write mode, parameters can be set and write to OTP. By writing to OTP, parameter settings are retained even after VCC is restarted.

Please note that OTP can only be written once. Please perform this procedure after performing pre-verification in "1. Register Setting Mode" and deciding all parameter settings.

In OTP write mode, the sequence is (1) Password input, (2) Parameter setting input, and (3) OTP write command input. (1) and (2) are the same sequence as "1. Register Setting Mode".

After the OTP write command, PROG is switched to "L", and OTP is written. After 10 ms or more, turn off VCC until V50 is 2 V or less, and then turn on VCC again. Please check the OTP write value in "2. Register Read Mode".

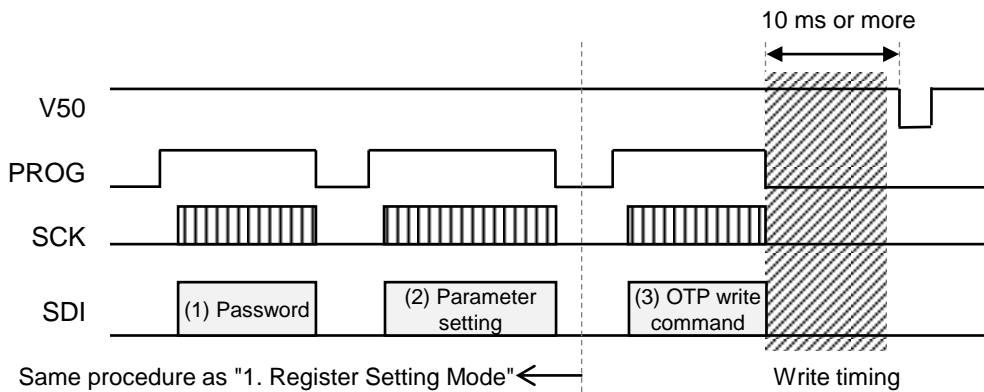


Fig. 4-38 OTP write sequence

(1) Password input

Input password = "0xD6A3" with PROG = "H" state. After inputting the password, please set PROG = "L".

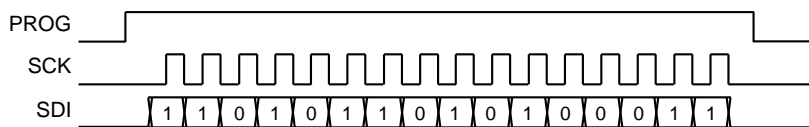


Fig. 4-39 OTP write password input

(2) Parameter setting input

Switch PROG to "H", input the address for which you want to set the parameters (7 bits, A6~A0), the register access type = "1" b0 (W)", and the data (8 bits, D7~D0), in that order. There is an automatic increment function to the next address, so when setting parameters to the next address, there is no need to input the next address. If you want to set parameters to an address other than the next address, input PROG = "L" and then input in the same procedure. After setting all parameters, set PROG = "L". This completes the register setting mode sequence.

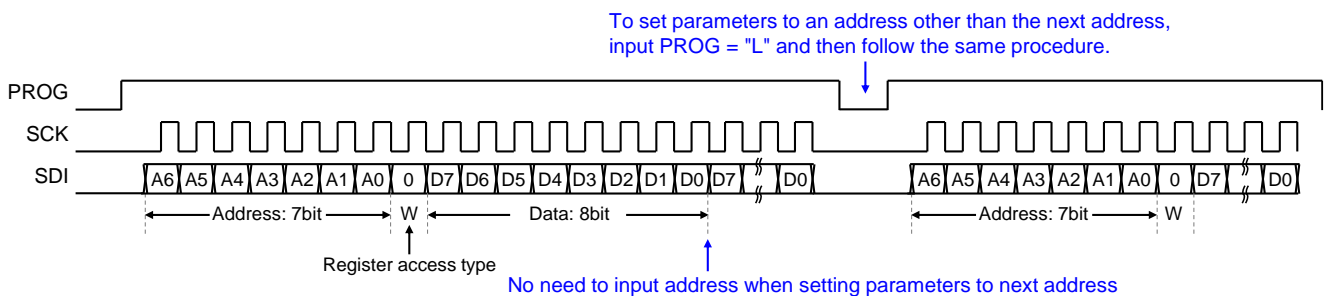


Fig. 4-40 OTP write parameter setting command

4.18 OTP Control Mode List (continued)

4.18.3 OTP Write Mode (continued)

(3) OTP write command

Switch PROG to "H" and input the OTP write command "0x0001". After inputting the OTP write command, set PROG to "L". After switching PROG to "L", writing to the OTP is performed. This completes the sequence for the OTP write mode.

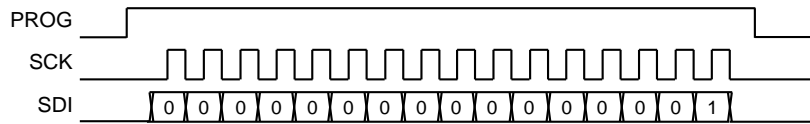


Fig. 4-41 OTP Write Command

4.18 OTP Control Mode List (continued)

4.18.4 OTP Read Mode

In OTP read mode, parameter settings written to the OTP can be read.

In OTP read mode, the sequence is (1) enter the password, (2) select the OTP read mode, and (3) read the register. After inputting the OTP read command in read mode selection, the OTP is read out and reflected in the register after PROG is switched to "L". Implement a register read to read out the settings written to the OTP.

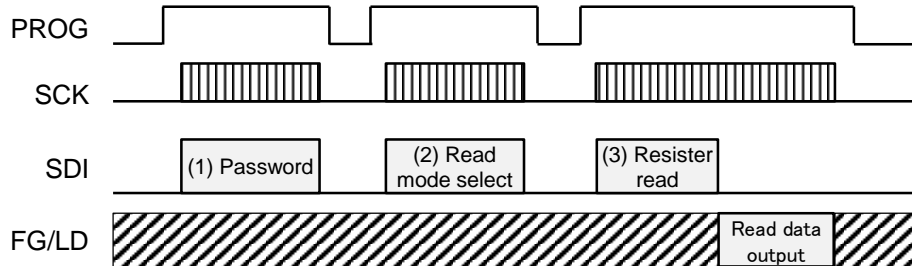


Fig. 4-42 OTP read sequence

(1) Password Input

Input password = "0xD6A3" with PROG = "H" state. After inputting the password, please set PROG = "L".

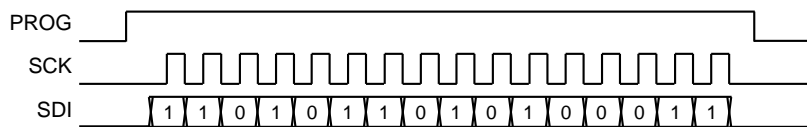


Fig. 4-43 OTP read password input

(2) Select OTP read mode

Switch PROG to "H" and input the OTP read command "0x0051". After inputting the OTP read command, set PROG to "L". After switching PROG to "L", OTP reading will be performed. It takes 100µs for the OTP read to complete. Please allow a wait time of at least 100µs before reading the register.

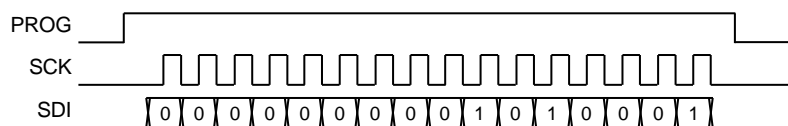


Fig. 4-44 OTP read command

4.18 OTP Control Mode List (continued)

4.18.4 OTP Read Mode (continued)

(3) Register read

Switch PROG to "H", input the address (7 bits, A6~A0) for register read, and register access type = "1' b1 (R)" in that order, and data (8 bits, D7~D0) will be output from FG / LD. There is an automatic increment function for the next address, so there is no need to input the next address when reading the register of the next address. If a register other than the next address to be read, input PROG = "L" and then input it in the same way. After completing the register read, set PROG = "L". This completes the sequence for OTP read mode.

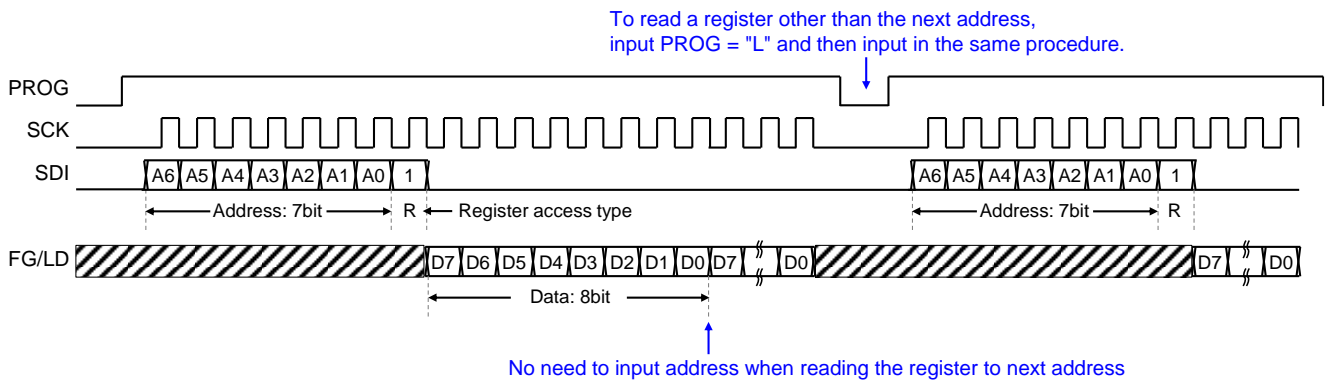


Fig. 4-45 OTP read parameter setting command

4.18 OTP Control Mode List (continued)

4.18.5 OTP Margin Check Mode

In OTP margin check mode, the output value of the data written to the OTP can be checked. In OTP margin check 1, the written data of uncut OTP are to be checked, and in OTP margin check 2, the written data of cut OTP are to be checked. The expected value of an uncut OTP is 0, and the expected value of a cut OTP is 1. In OTP margin check mode, the sequence is (1) enter a password, (2) select read mode, and (3) read a register. In read mode, after inputting an OTP read command and switching PROG to "L", the OTP is read and reflected in the register. A register read is performed to read the settings written to the OTP.

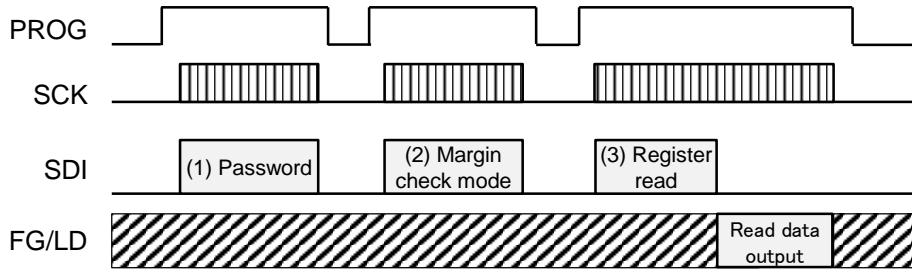


Fig. 4-46 OTP margin check sequence

(1) Password input

Input password = "0xD6A3" with PROG = "H" state. After inputting the password, please set PROG = "L".

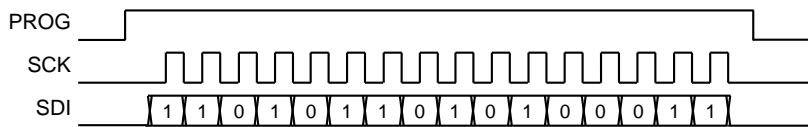


Fig. 4-47 OTP margin check password input

(2) Select margin check mode

Switch PROG to "H" and input "0x0041" for OTP margin check 1, or "0x0061" for OTP margin check 2. After inputting the OTP margin check command, set PROG to "L". After switching PROG to "L", OTP reading will be performed. It takes 100µs for the OTP read to complete. Please allow a wait time of at least 100µs before reading the register.

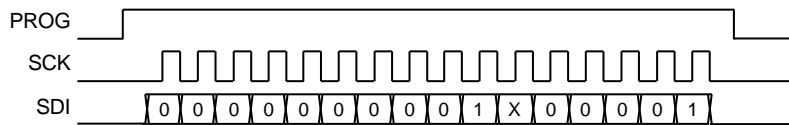


Fig. 4-48 OTP margin check command

4.18 OTP Control Mode List (continued)

4.18.5 OTP Margin Check Mode (continued)

(3) Register read

Switch PROG to "H", input the address (7 bits, A6~A0) for register read, and register access type = "1' b1 (R)" in that order, and data (8 bits, D7~D0) will be output from FG / LD. There is an automatic increment function for the next address, so there is no need to input the next address when reading the register of the next address. If a register other than the next address is to be read, input PROG = "L" and then input it in the same way. After completing the register read, set PROG = "L". This completes the OTP write mode sequence.

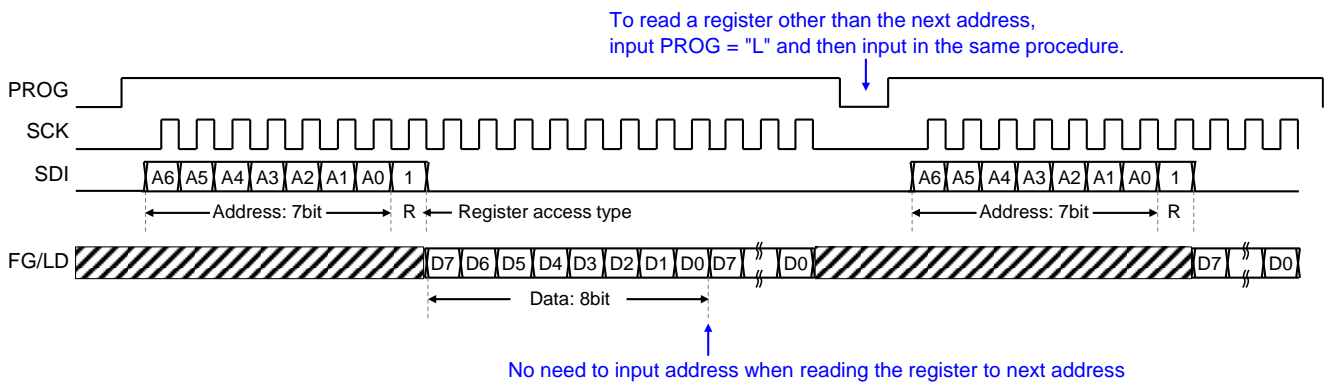


Fig. 4-49 OTP margin check read command

■ (Reference) Timing Chart

SCK and SDI timing chart

Make sure that data can be captured by shifting the timing of SDI switching and SCK input. It is recommended such that the transition SDI of data falls on the falling edge of SCK so that it is captured on the rising edge of SCK. The following figure is an example of transitioning SDI at the falling edge of SCK.

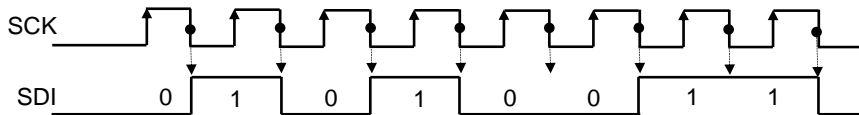


Fig. 4-50 Example of OTP data setting timing

SCK and FG / LD timing chart

Make sure that the data can be captured by shifting the timing of FG / LD switching and SCK input. It is recommended to take in the FG / LD output data at the falling edge of SCK. The timing chart below is an example of data output at the falling edge of SCK being captured at the rising edge of SCK. The FG / LD terminal outputs the 1st bit of data before the SCK input, and the 2nd bit of data at the first SCK input. Please note that the FG / LD terminal is an open drain output, so if the external CR is large and the SCK input frequency is high, it may not be possible to read correctly.

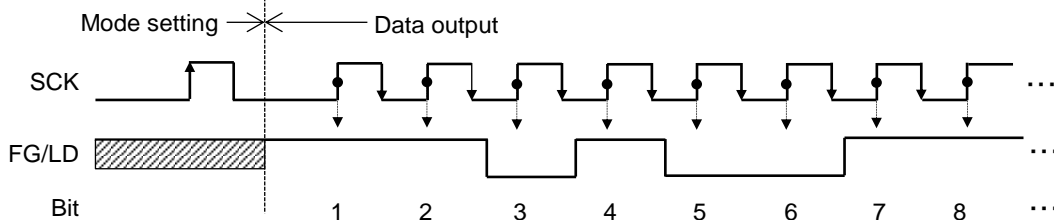


Fig. 4-51 Example of OTP data read timing

4.19 OTP Write Inspection Flow

Inspection of normal OTP writing is required before shipment. Please perform the inspection according to the flow below.

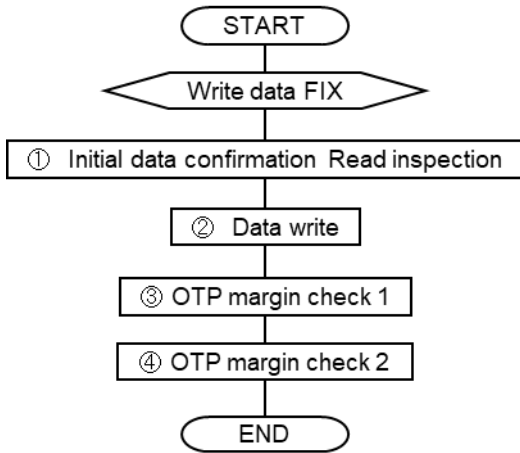


Fig. 4-52 OTP inspection flow

	Item	Detail	Expected value
①	Initial data confirmation Read inspection	Confirm that all BITs are uncut before writing.	All data = 0
②	Data write	Data write execution.	—
③	OTP margin check 1	Mainly check write data uncut OTP output value	Uncut OTP data = 0
④	OTP margin check 2	Mainly check the write data disconnected OTP output value	Disconnected OTP data = 1

Judgment criteria

If the reading results of ①, ③, and ④ are different from the expected values, please judge it as a defective product.

4.20 OTP Program Environment and Precautions for Using OTP

- Please check the voltage waveform of the V50 pin at the OTP write timing, and adjust the V50 capacitance value so that the V50 voltage is within the range of No. 2 in the table below.
- Please perform OTP cutting program verification (Total: >10000 bits) before mass production.
- If a defect of 1% or more occurs, there may be a program defect.
- Add a bypass capacitor (0.1 μ F or more) to the V50 pin as close to the IC as possible.
- Be sure not to rewrite to the data address that has been written once.
- When performing OTP writing for set evaluation and mass production, be sure to write PROTECT BIT.

Note) If OTP is used under conditions other than the stated above, an OTP write error may occur. Please perform sufficient verification before using it.

No.	Item	Symbol	Condition	Reference value			Unit
				Min.	Typ.	Max.	
1	VCC voltage when writing	V _{CCPROM}	—	8	-	76	V
2	V50 voltage when writing	V _{50PROM}	Described below Fig.4-53	4.6	5	5.4	V
3	Instantaneous power supply current during writing	I _p	—	—	—	100	mA

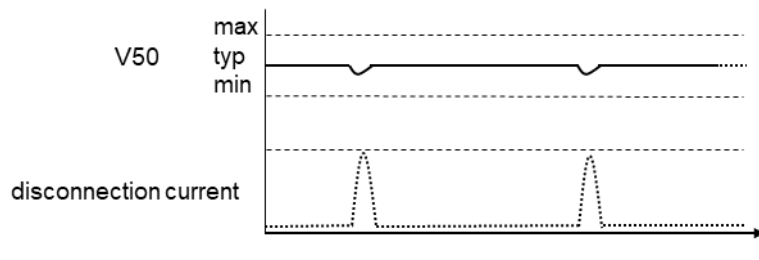


Fig. 4-53 V50 voltage during OTP write

4.21 Protection Function

To ensure safe operation, the device is equipped with protection against V50 undervoltage, VCC undervoltage, VCC overvoltage, overtemperature and motor lock.

Function	Operate	Release	Note
V50 undervoltage lock out	3.2V	3.3V	When V50 is less than UVLO threshold voltage, power OFF
VCC undervoltage lock out	6.2V (V _{LVD_H} = GND) 18V (V _{LVD_H} = V50)	6.7V (V _{LVD_H} = GND) 20V (V _{LVD_H} = V50)	When VCC is less than UVLO threshold voltage, power OFF.
VCC overvoltage protection (Clamp)	External Zener diode voltage + 10.8V + VGS of external MOSFET or more	VCC overvoltage protection operating voltage or less	<p>By connecting an external Zener diode D_{CLAMP} between the CLAMP pin and the VCC pin, the VCC voltage is limited to above the VCC clamp operating voltage.</p> <p>If the VCC overvoltage protection function is not used, connect the CLAMP pin to GND. A power isolation diode between VCC and VM is not required.</p>
Thermal shutdown (Junction temperature)	160°C	135°C	When the TSD protection is activated, power OFF
Motor lock protection	When no hall signal continues for more than the Motor lock detection time.	<ul style="list-style-type: none"> • Turn on the VCC power supply again • Restart by VSP • After Motor lock protection release time progress 	If no Hall signal continues for more than the set time, the motor stops, power OFF

5. PACKAGE INFORMATION

5.1 Outline Drawing

QFN32L 4x4mm², Thickness 0.80mm, Lead Pitch 0.40mm,
Lead Length 0.35mm, EP Size 2.8x2.8mm²

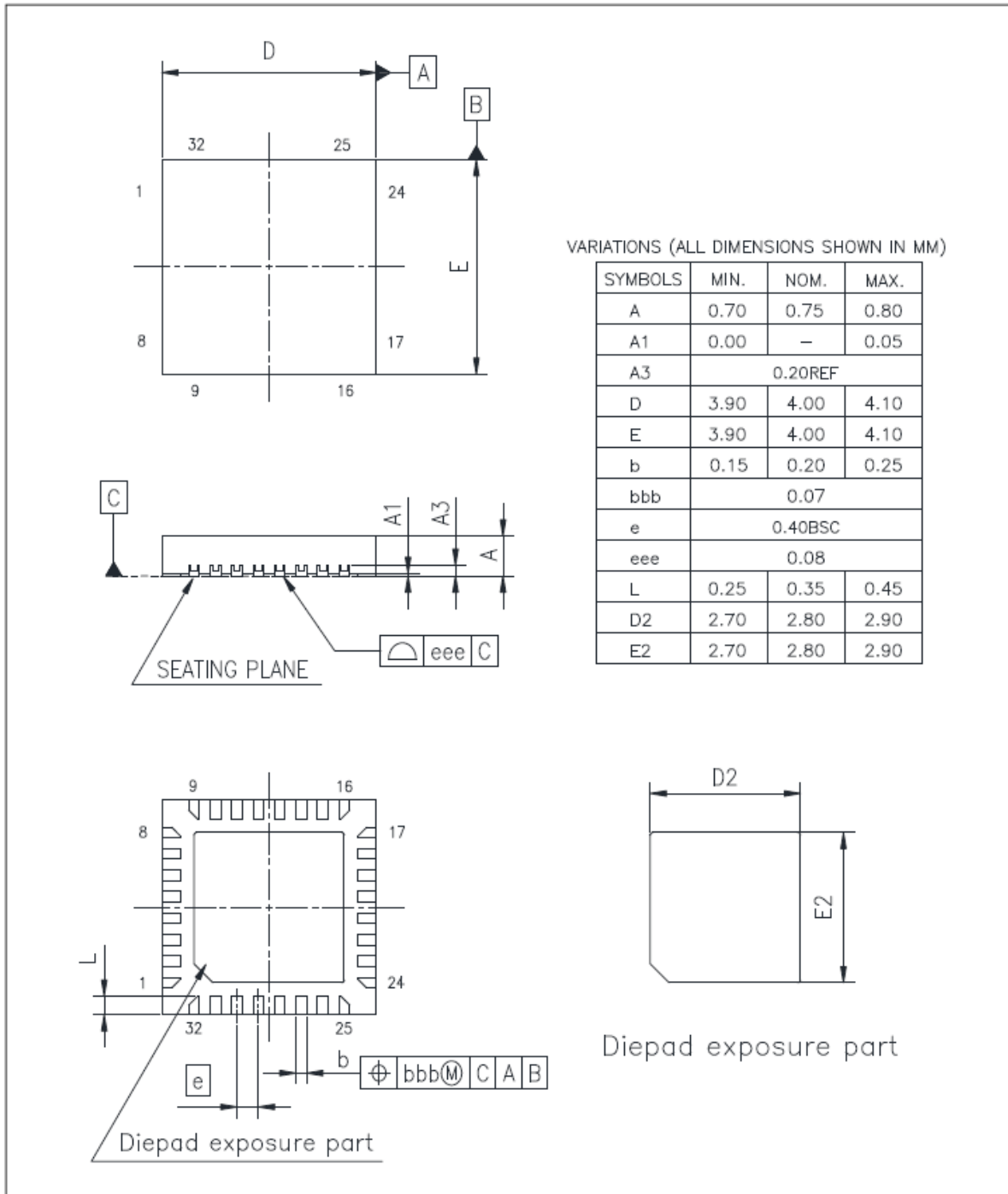


Fig. 5-1 Outline Drawing of package

USAGE NOTES

1. It is the customer's responsibility to confirm safety, including reliability, for each set when expanding models or using the product in a new set.
2. When designing an application system using an IC, it is the customer's responsibility to check the precautions carefully. Be sure to read the notes on explanations and usage notes in the text.
3. This IC is intended to be used for general consumer equipment.
Customers who are considering using the product in the following applications where special quality and reliability are required and failure or malfunction may directly threaten human life or harm the human body, and our intended standard. If you plan to use the product for purposes other than those intended, please contact our sales representative in advance. Please note that we are not responsible for any damage caused by using the product without contacting us.
 - (1) Space equipment (artificial satellites, rockets, etc.)
 - (2) Control equipment for transport vehicles (automobiles, aircraft, trains, ships, etc.)
 - (3) Medical devices intended for life support
 - (4) Submarine relay equipment
 - (5) Power plant control equipment
 - (6) Disaster prevention and crime prevention equipment
 - (7) Weapons
 - (8) Others: Applications requiring reliability equivalent to (1)-(7)
4. This IC is not intended for use in automotive applications, nor is it designed to be used in an automotive environment, unless specified as an automotive product by our company.
We do not take any responsibility for any damages caused to customers or third parties by using this IC in automotive applications without our prior written consent.
5. When using this IC, thoroughly investigate the laws and regulations such as the RoHS Directive, which regulates the inclusion and use of specific substances, and use it in compliance with such laws and regulations.
We are not responsible for any damage caused by your non-compliance with applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (Printed Circuit Board), it might be damaged.
7. Pay close attention to the pattern layout to prevent damage due to short circuit between terminals. Please refer to the pin description for the pin arrangement of this IC.
8. This IC may be damaged if its pins are opened, so carefully check the PCB before applying power.
9. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC.
Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
10. Take notice in the use of this IC that it might be damaged and be emitted a little smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), output-to-output-pin short (load short), or leakage between pins, etc.
Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
11. The protection circuit is for maintaining safety against abnormal operation. Therefore, please design so that the protection circuit will not operate in normal use.
When sudden voltage or current change is applied to the pin, it may exceed the designated voltage and current level and therefore, customer shall perform sufficient evaluation and verification to ensure these are not exceeded in the usage.
Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged and emit smoke before the thermal protection circuit could operate.
12. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the IC might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
13. Please verify the risks due to failure of external components.
14. Connect the metallic plate (fin) on the back side of the IC to the GND potential. The thermal resistance and electrical characteristics are guaranteed only when the metallic plate (fin) is connected with the GND potential.

USAGE NOTES(continued)

15. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, pin stress and mechanical stress) at the time of handling, mounting or at customer's process.
16. Apply power supply with low impedance to VCC and connect bypass capacitor near to the IC.
17. After VCC is input, if the VCC voltage drops due to motor driving while VCC rises to the specified voltage, it may not start normally. Therefore, please fully evaluate and consider the current capability of the power supply.

Revision History

Date	Revision	Description
2024.7.8	1.00	1. initially issued.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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