Mini CAN FD System Basis Chip

ATA6500 / ATA6501 / ATA6502 / ATA6503 / ATA6504 / ATA6505

Description

The ATA650X is a CAN FD System Basis Chip (SBC) with a fully integrated high-speed CAN FD transceiver that interfaces a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus and a low-drop voltage regulator (5V/150 mA). The transceiver is designed for high-speed Classical CAN and CAN FD (up to 8 Mbit/s) applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller. The combination of voltage regulator and CAN FD transceiver makes it possible to develop simple but powerful nodes in CAN bus systems.

The various operating modes along with the dedicated fail-safe features make the ATA650X SBC an excellent choice for all types of Classical CAN and CAN FD networks.

Microchip's SBC is available in very small, space-saving packages with wettable flanks for automated optical inspection capability.

Features

CAN FD Transceiver

- CAN FD Transceiver Fully Compliant to ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5
- Highly Symmetrical Transmitter
- Communication Speed up to 8 Mbit/s
- Autonomous Bus Biasing According to ISO 11898-2:2024
- Very Low Sleep Current Consumption (typical 15 µA)
- Differential Receiver with Wide Common-Mode Range
- Functional Behavior Predictable Under All Supply Conditions
- VIO Input Allows for Direct Interfacing with 1.8V, 3.3V and 5V Microcontrollers
- Transceiver Disengages from the Bus when not powered
- RXD Recessive Clamping Detection
- Transmit Data (TXD) Dominant Time-Out Function
- Receive Only Mode for Node Diagnostics and Fault Confinement
- CANH/CANL Short Circuit and Overtemperature Protection
- High Electrostatic Discharge (ESD) Handling Protection on the Bus Pins
- Bus Pins Protected Against Transients in Automotive Environments
- Undervoltage Detection on VCC Pin with Open Drain Reset Output (NRES Pin, 4 ms Reset Time)
- Undervoltage Detection on VIO Pin
- INH Output to Control an External Load, e.g., Voltage Regulator
- High-Voltage WAKE Input Pin
- Remote Wake-Up Capability through CAN Bus (Wake-Up Pattern (WUP) According to ISO 11898-2:2024)
- Wake-Up Source Recognition
- CAN FD Transceiver Fully Compliant to SAE J2962-2

- ESD according to IEC 62228-3, following IEC61000-4-2: (330Ω/150 pF) - Pins CANH, CANL, VS, WAKE ± 6 kV

Voltage Regulator

- Integrated 5V, 150 mA Low Dropout Voltage Regulator
  - ± 2% Accuracy
  - Current limitation above 150 mA
  - Max RDSON of output transistor 5Ω
  - Short-Circuit protection
  - Undervoltage detection
  - Overvoltage protection
  - Overtemperature protection

Functional Safety Support

- ISO 26262:2018 Functional Safety Ready up to ASIL B
- IEC 61508:2010 Functional Safety Ready up to SIL 2

Automotive Qualification

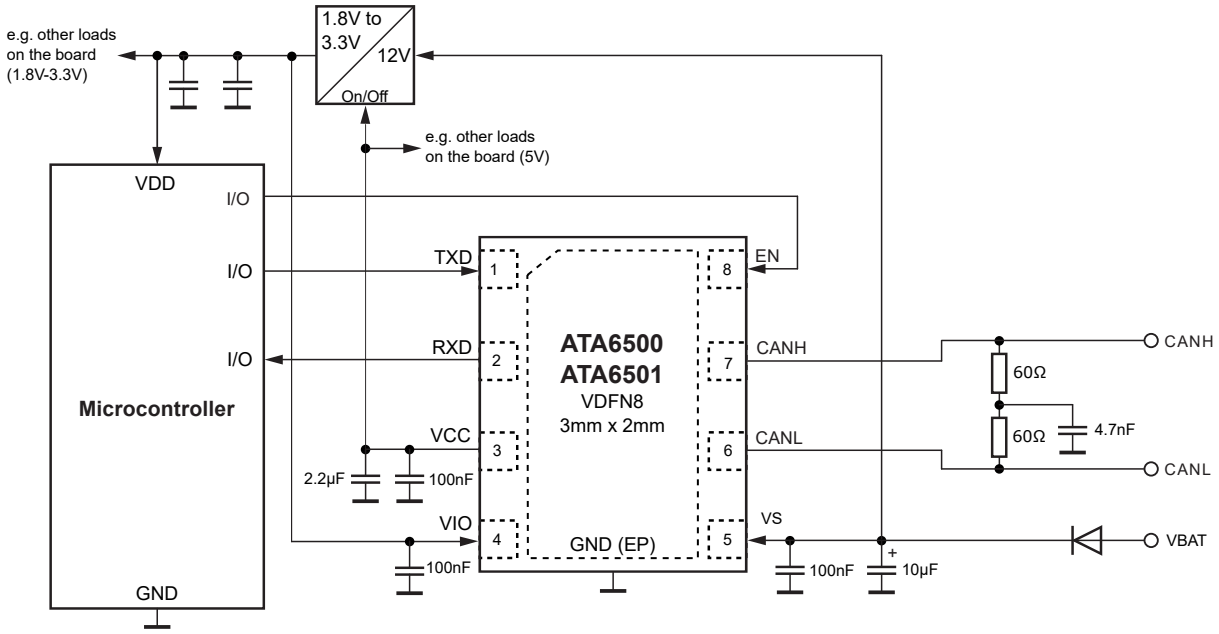
- Fulfills the OEM Hardware Requirements for CAN in Automotive Applications, Rev. 1.3
- AEC Q100 Qualified
- Ambient Temperature Grade 0:
  - T_{amb} = -40°C to +150°C
- Available Packages: VDFN8, VDFN10 and VDFN14 with Wettable Flanks (Moisture Sensitivity Level 1)

Applications

- Body Electronics and Lighting
- Automotive Infotainment
- Powertrain Systems
- Advanced Driver Assistance Systems (ADAS)
- Photovoltaic
- E-bike

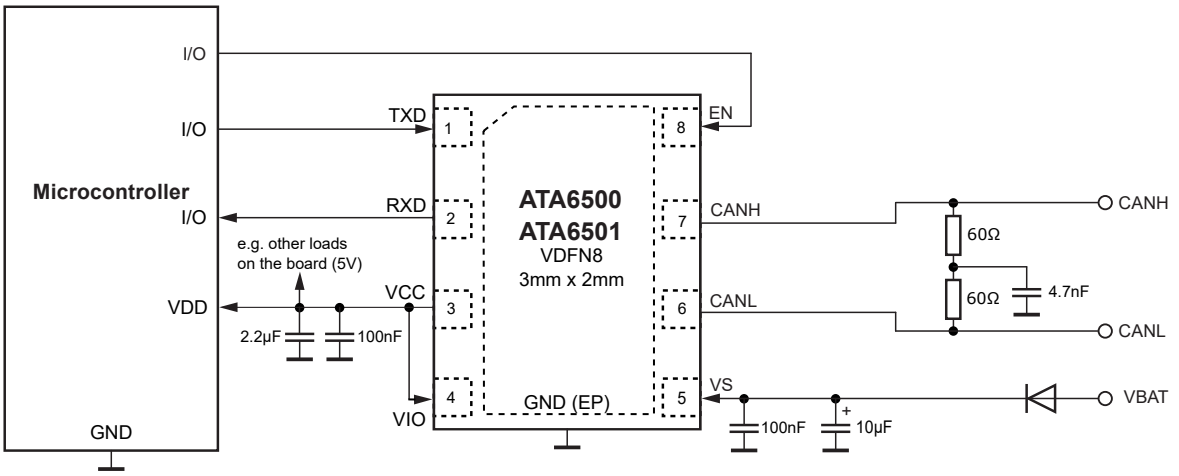
1. Typical Application

Figure 1-1. Typical Application Circuit ATA6500/ATA6501, 1.8V/3.3V MCU



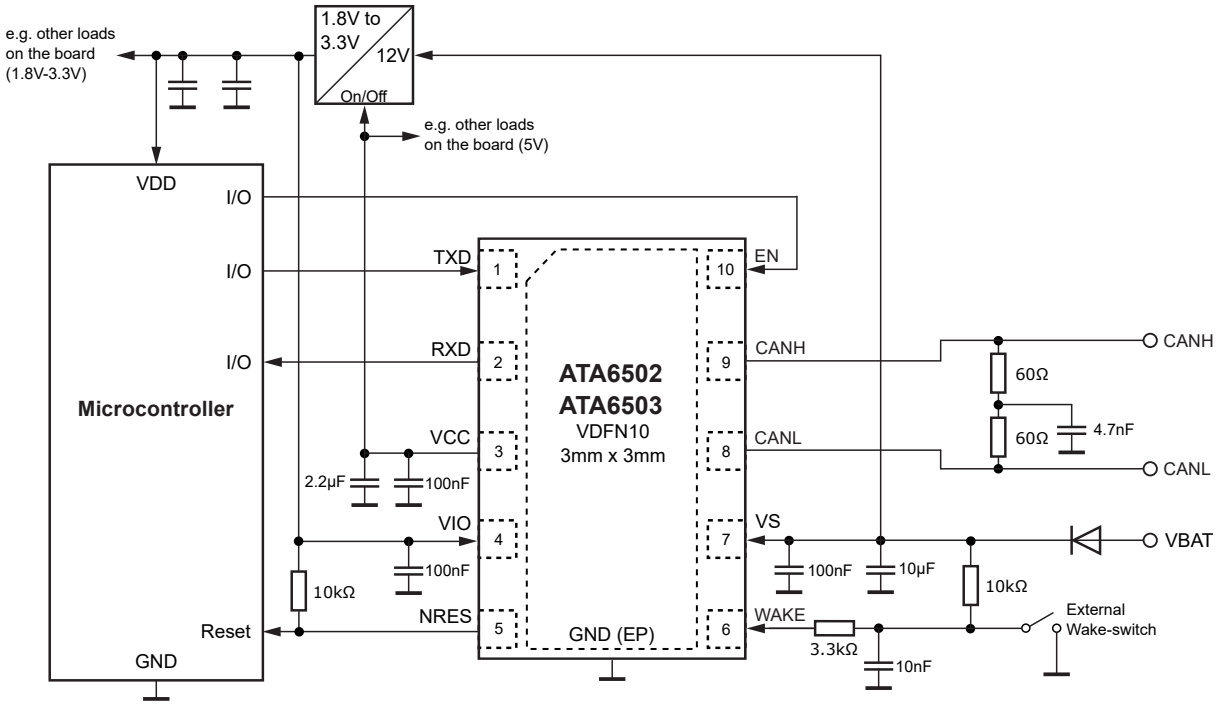
Note: The exposed thermal pad must always be connected to GND.

Figure 1-2. Typical Application Circuit ATA6500/ATA6501, 5V MCU



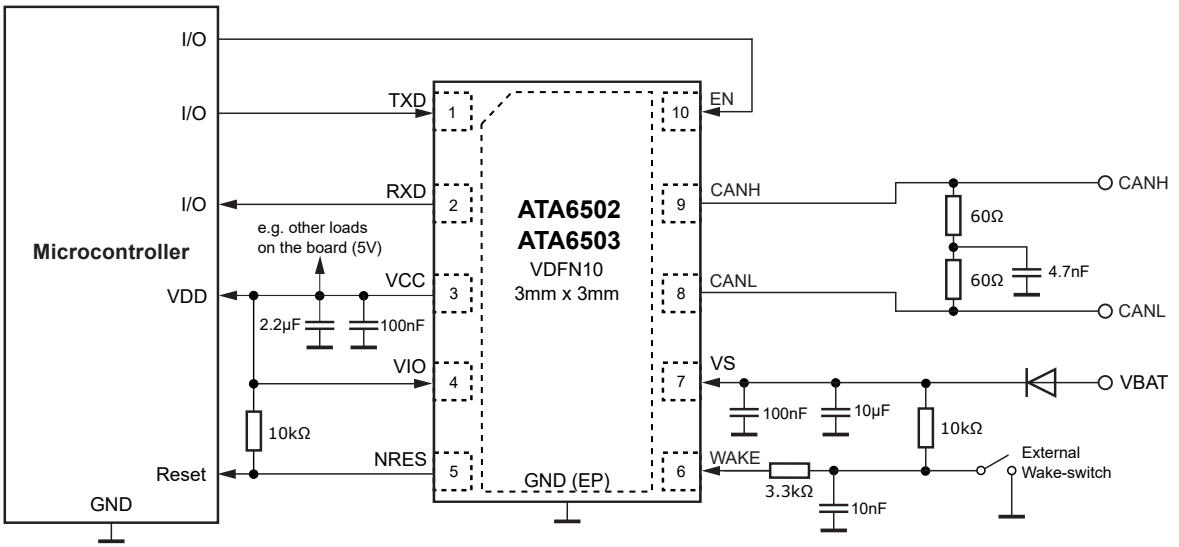
Note: The exposed thermal pad must always be connected to GND.

Figure 1-3. Typical Application Circuit ATA6502/ATA6503, 1.8V/3.3V MCU



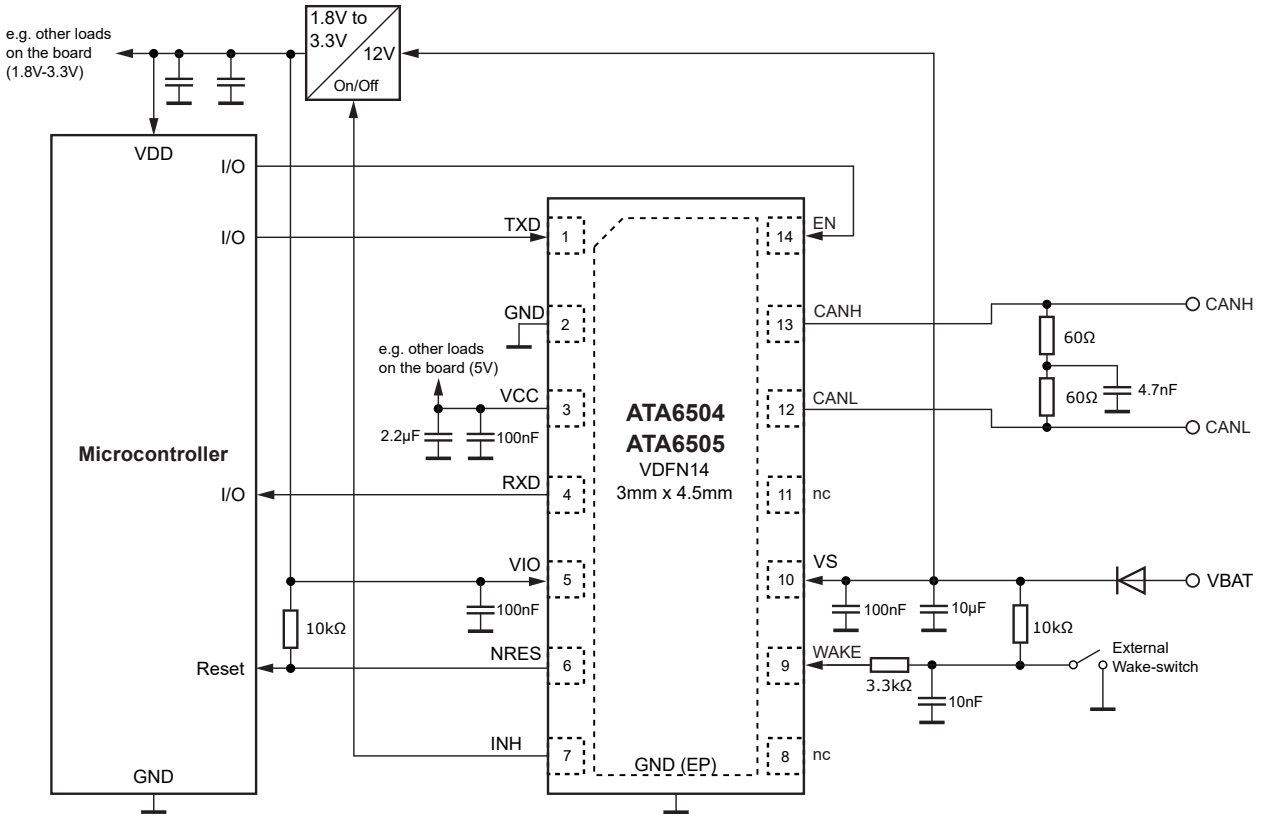
Note: The exposed thermal pad must always be connected to GND.

Figure 1-4. Typical Application Circuit ATA6502/ATA6503, 5V MCU



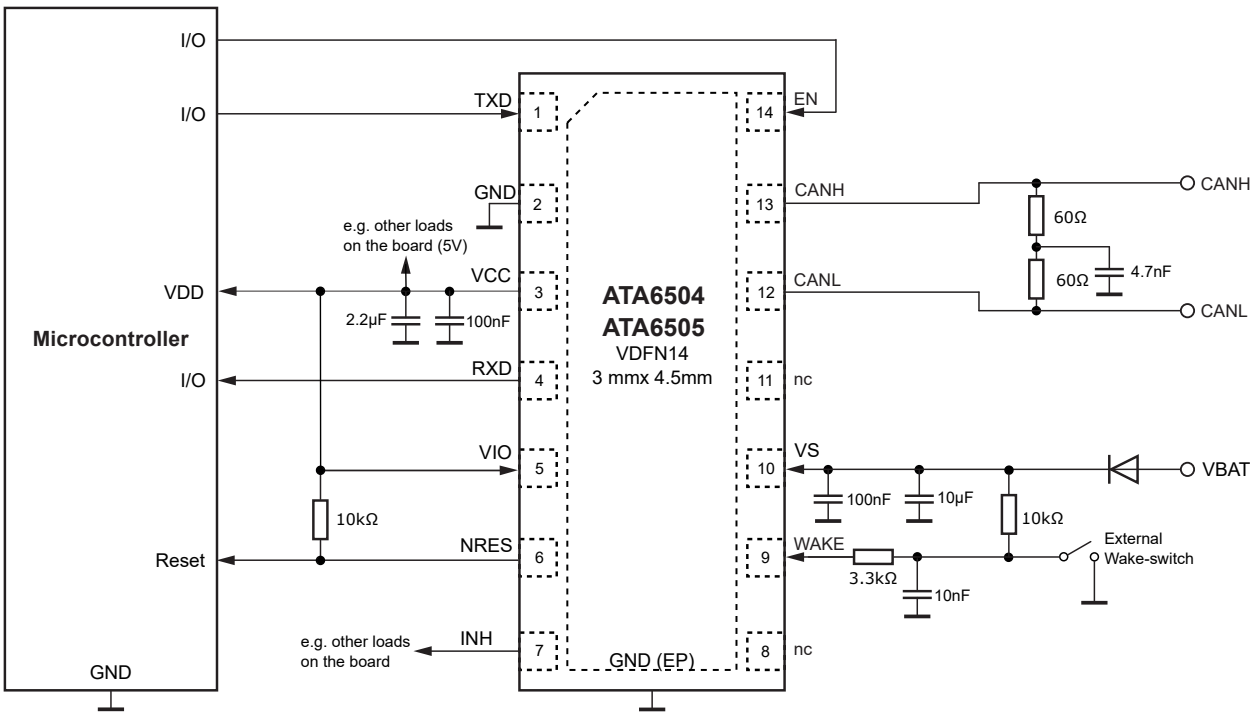
Note: The exposed thermal pad must always be connected to GND.

Figure 1-5. Typical Application Circuit ATA6504/ATA6505, 1.8V/3.3V MCU



Note: The exposed thermal pad must always be connected to GND.

Figure 1-6. Typical Application Circuit ATA6504/ATA6505, 5V MCU



2. Product Family

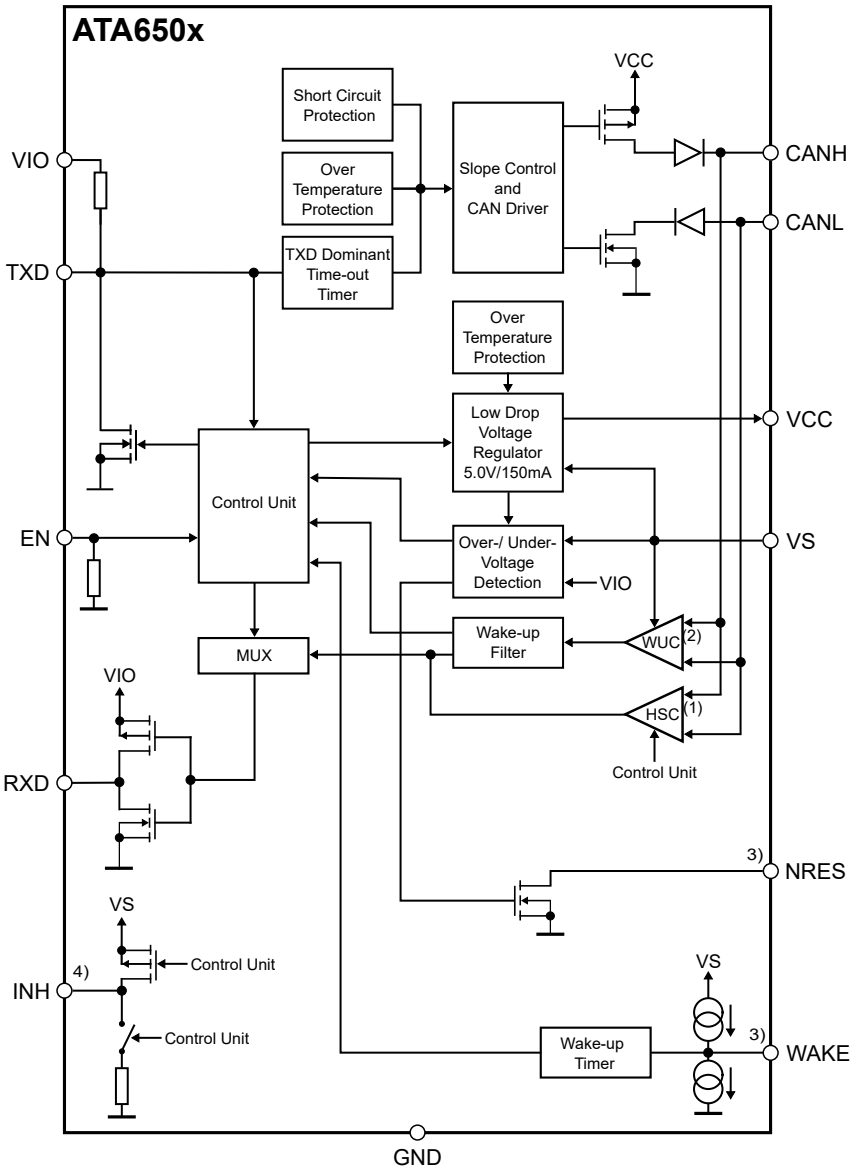
The device names, features, and package types are listed in the following table. All devices integrate a high-speed CAN FD transceiver and a low-dropout voltage regulator (5V/150 mA).

Table 2-1. ATA650X Family Members

Device	Grade 0	VIO	NRES	INH	WAKE	Packages
ATA6500	x	1.8V/5V				VDFN8
ATA6501	x	3.3V/5V				VDFN8
ATA6502	x	1.8V/5V	x		x	VDFN10
ATA6503	x	3.3V/5V	x		x	VDFN10
ATA6504	x	1.8V/5V	x	x	x	VDFN14
ATA6505	x	3.3V/5V	x	x	x	VDFN14

3. Block Diagram

Figure 3-1. Simplified Block Diagram



Notes:

1. High-Speed Comparator.
2. Wake-Up Comparator.
3. 10-pin and 14-pin packages.
4. 14-pin package.

4. Pin Configuration

Figure 4-1. Pin Configuration ATA6500 and ATA6501 (VDFN8)

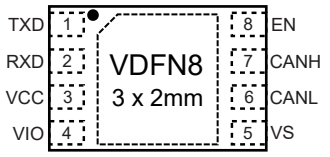


Table 4-1. Pin Description VDFN8

ATA6500/1	Symbol	Function
1	TXD	Transmit Data Input Pin
2	RXD	Receive Data Output Pin
3	VCC	Voltage Regulator Output Pin (5V/150 mA)
4	VIO	Supply Voltage for the I/O Pins
5	VS	Battery Supply Voltage Pin
6	CANL	Low-Level CAN Bus Line
7	CANH	High-Level CAN Bus Line
8	EN	Enable Control Input Pin
9	GND/Heat Slug	Ground; exposed Thermal Pad

Figure 4-2. Pin Configuration ATA6502 and ATA6503 (VDFN10)

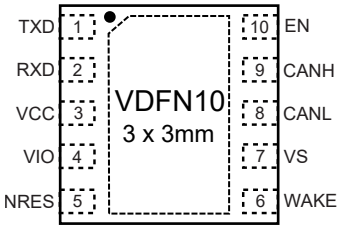


Table 4-2. Pin Description VDFN10

ATA6502/3	Symbol	Function
1	TXD	Transmit Data Input Pin
2	RXD	Receive Data Output Pin
3	VCC	Voltage Regulator Output Pin (5V/150 mA)
4	VIO	Supply Voltage for the I/O Pins
5	NRES	Open Drain Reset Output Pin, low active
6	WAKE	Local Wake-Up Input. Connect directly to the VS pin or the GND pin, if not used.
7	VS	Battery Supply Voltage Pin
8	CANL	Low-Level CAN Bus Line
9	CANH	High-Level CAN Bus Line
10	EN	Enable Control Input Pin
11	GND/Heat Slug	Ground; exposed Thermal Pad

Figure 4-3. Pin Configuration ATA6504 and ATA6505 (VDFN14)

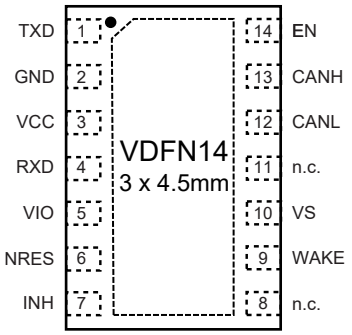


Table 4-3. Pin Description VDFN14

ATA6504/5	Symbol	Function
1	TXD	Transmit Data Input Pin
2	GND	Ground Pin
3	VCC	Voltage Regulator Output Pin (5V/150 mA)
4	RXD	Receive Data Output Pin
5	VIO	Supply Voltage for the I/O Pins
6	NRES	Open Drain Reset Output Pin, low active
7	INH	VS related Inhibit Output switch for controlling external loads, e.g., voltage regulators
8	n.c.	Not Connected
9	WAKE	Local Wake-Up Input. Connect directly to the VS pin or the GND pin, if not used.
10	VS	Battery Supply Voltage Pin
11	n.c.	Not Connected
12	CANL	Low-Level CAN Bus Line
13	CANH	High-Level CAN Bus Line
14	EN	Enable Control Input Pin
15	GND/Heat Slug	Ground; exposed Thermal Pad

4.1 Battery Supply Voltage Pin (VS)

This is the power supply pin. This pin is usually connected to the battery through a serial diode for reverse battery protection. This pin sustains standard automotive conditions, such as 40V during load dump. An undervoltage detection circuit is implemented to avoid a malfunction or false bus messages. After switching ON the VS pin, the IC starts in Reset mode, the VCC voltage regulator and the INH output (only ATA6504/5) are switched ON; after the VCC voltage is settled, the device switches into Standby mode.

4.2 Ground Pin (GND)

The device does not affect the CAN bus in the event of a GND disconnection.

4.3 Voltage Regulator Output Pin (VCC)

The 5V voltage regulator is capable of driving loads up to 150 mA: supplying the CAN FD transceiver, the microcontroller (only for 5V µCs), and other ICs/loads on the PCB. It is protected against overload by means of current limitation and overtemperature shutdown. The output voltage is continuously monitored while the regulator is ON. Furthermore, when a VCC overvoltage condition is detected, the regulator switches OFF automatically. If the VCC voltage drops below a defined threshold $V_{VCC\_th\_UV\_DOWN}$, the NRES output pin is asserted (only ATA6502/3/4/5) and the device enters Reset mode.

4.4 Supply Pin for I/O Level Adapter (VIO)

This is the supply pin for the digital input/output pins. This pin should be connected to the microcontroller's supply voltage to adjust the signal levels of pins TXD and RXD to the I/O levels of the microcontroller. The device monitors the VIO pin for undervoltage.

The ATA650X device is available in two VIO variants:

- ATA6501/3/5: VIO undervoltage threshold for 3.3V and 5V µC (V_{VIO_UV})
- ATA6500/2/4: VIO undervoltage threshold for 1.8V and 5V µC (V_{VIO_UV})

For a 5V microcontroller, the VIO pin should be connected to the VCC pin and the VCC voltage is the supply for the CAN FD Transceiver and for the microcontroller.

4.5 CAN Bus Pins (CANH and CANL)

The CANL pin is a low-side driver to GND, and the CANH pin is a high-side driver to VCC. In Normal mode and if TXD is high, the CANH and CANL drivers are OFF, and the voltage at CANH and CANL is $V_{VCC}/2$, approximately 2.5V, provided by the internal bus biasing circuitry. This state is called recessive.

When TXD is low, CANL is pulled towards GND and CANH towards VCC, creating a differential voltage on the CAN bus. This state is called dominant.

In Standby and Sleep mode, the CANH and CANL drivers are OFF. If the device is in OFF mode, CANH and CANL are highly resistive with extremely low leakage current to GND, making the device ideally passive.

The CANH and CANL pins have integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients. The CANH and CANL bus outputs are short-circuit protected against GND or a positive supply voltage and are also protected against overtemperature conditions.

4.6 Transmit Data Input Pin (TXD)

In Normal mode, this input pin controls the CAN bus state. In the application, this pin is connected to the microcontroller transmit terminal. The TXD pin has an internal pull-up resistor towards VIO to ensure a safe defined recessive driver state in case this pin is left floating. When TXD is high or floating, the CANH and CANL drivers are OFF, setting the bus into the recessive state. The TXD pin must be pulled to logic low in order to activate the CANH and CANL drivers, and set the bus to the dominant state. A TXD dominant time-out timer is started when the TXD pin is set to low. If the low state on the TXD pin persists for longer than $t_{to(dom)}$, the transmitter is disabled, releasing the bus lines to the recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set high for longer than $t_{TX\_resume\_TXDOUT}$. The transmitter is also disabled if pin TXD is held low (e.g., by a short circuit to GND), while the device is switched into Normal mode; therefore, the bus lines are in the recessive state. The transceiver remains in this state until pin TXD is set to high.

In Standby mode, the TXD pin is used as an output signaling, together with the RXD pin, the wake-up source, or a VS undervoltage.

4.7 Receive Data Output Pin (RXD)

In Normal and Receive Only mode, this pin reports the state of the CAN bus to the microcontroller. In the application, this pin is connected to the microcontroller receive terminal. RXD is high when the bus is recessive. When the bus is dominant, RXD is low.

The output is a push-pull structure; the high-side is connected to VIO and the low-side to GND.

In Standby mode, the RXD pin signals, together with the TXD pin, the wake-up source, or a VS undervoltage.

An RXD recessive clamping function (see section 5.2.2. RXD Recessive Clamping) is implemented. This fail-safe feature prevents the controller from sending data on the bus if the RXD line is clamped to high.

4.8 Inhibit Output Pin (INH - only ATA6504 and ATA6505)

The inhibit output pin provides an internal switch towards the VS pin and is used to control external voltage regulators or other external loads. If the device is in Normal, Receive Only, Reset or Standby mode, the inhibit high-side switch is turned ON. When the device is in Sleep mode, the inhibit switch is turned OFF, thus disabling the connected external voltage regulators or other connected external devices. A pull-down is implemented to ensure a defined level when the inhibit switch is turned OFF.

A wake-up event on the CAN bus, or at the WAKE pin, switches the INH pin to the VS level. After a system power-up (VS rises from zero), the INH pin switches to the VS level automatically.

4.9 Wake Input Pin (WAKE - only ATA6502, ATA6503, ATA6504 and ATA6505)

This high-voltage input pin is used for waking up the device from Sleep mode. It is usually connected to an external switch in the application to generate a local wake-up. If the WAKE pin is not needed in the application, it should be connected to VS or GND to ensure optimal EMI performance.

The WAKE pin has a special design structure and is triggered by a low-to-high or a high-to-low transition, directly followed by a stable level for a given time period (> t_{local_wu}), which results in a local wake-up request. This feature allows for maximum flexibility when designing a local wake-up circuit.

An internal filter is implemented to avoid a false wake-up event due to noise. A serial resistor should be inserted in order to limit the input current mainly during transient pulses and ESD. The recommended resistor value is 3.3 kΩ. An external 10 nF capacitor is recommended for better EMC and ESD performance (see typical application circuit).

The local wake-up request switches the device into Reset and then to Standby mode and is signaled by a high level at the RXD pin and a low level at the TXD pin.

To reduce the current consumption during Low-Power mode, the internal pull-up/pull-down circuit follows the logic level at the WAKE pin:

- A high level on the pin is followed by an internal pull-up towards VS.
- A low level on the pin is followed by an internal pull-down towards GND.

4.10 Enable Input Pin (EN)

The enable input pin controls the operating mode of the device, together with the TXD pin (see Figure 5-1). An internal pull-down resistor is implemented to ensure a safe defined state in case this pin is left floating. The ESD protection structure is not connected to VIO, therefore the device can be woken up via the EN pin, even if the VIO voltage is not present.

4.11 Reset Output Pin (NRES - only ATA6502, ATA6503, ATA6504 and ATA6505)

The NRES pin is an open drain output and active low. The ESD structure is not connected to VIO, therefore, the NRES pin can be connected with other outputs of external reset sources in order to have a wired OR connection of these independent reset sources. If the VCC voltage falls below the undervoltage detection threshold $V_{VCC\_th\_UV\_DOWN}$ for longer than t_{res_f}, NRES is asserted. NRES stays low even if V_{VCC} = 0V because NRES is internally driven from the VS voltage. If the VS voltage ramps down, NRES stays low until V_{VS} < 1.5V and then becomes highly impedant.

When VCC ramps up, the implemented delay keeps NRES low for t_{Reset} after VCC has reached the VCC undervoltage clear threshold voltage, $V_{VCC\_th\_UV\_UP}$.

5. Functional Description

The ATA650X high-speed CAN FD SBC offers a number of operating modes, diagnostic features and fail-safe features that enable enhanced system reliability and advanced power management.

5.1 Device Operation Modes

The control pins EN and TXD are used to select one of the five operating modes supported by the ATA650X. Figure 5-1 illustrates the different modes and mode transitions.

Figure 5-1. Operating Modes

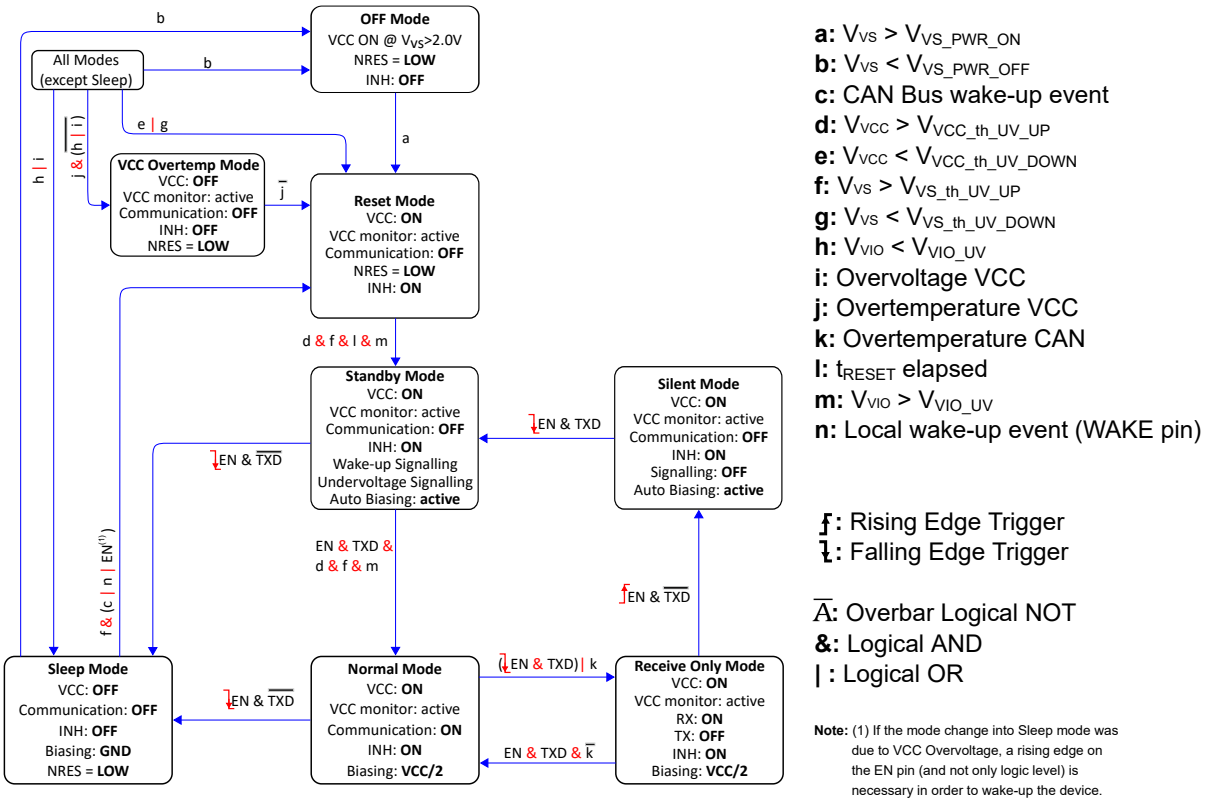


Table 5-1. Operating Modes

Operating Mode	CAN Transceiver	VCC	CANH	CANL	TXD	RXD	INH	NRES
Reset Mode	Off	On	Biased to GND	Biased to GND	High, if VIO present	High	On	Low
Standby Mode	Off	On	Autonomous bus biasing	Autonomous bus biasing	Signaling wake-up sources or VS undervoltage (If no wake-up source or VS undervoltage is signaled, the state is High High)		On	High ohmic
Silent Mode	Off	On	Autonomous bus biasing	Autonomous bus biasing	High	High	On	High ohmic
Normal Mode	On	On	Follows data transmission	Follows data transmission	Controlled by the ext. µC (high/low)	Reflects the CAN Bus	On	High ohmic

.....continued

Operating Mode	CAN Transceiver	VCC	CANH	CANL	TXD	RXD	INH	NRES
Receive Only Mode	Transmitter = Off Receiver = On	On	Follows data transmission	Follows data transmission	High	Reflects the CAN Bus	On	High ohmic
Sleep Mode	Off, wake-up detection active	Off	Biased to GND	Biased to GND	Follows VIO (pull-up to VIO)	High, if VIO present	Off (pull-down to GND)	Low
VCC Overtemperature Mode	Off	Off	Biased to GND	Biased to GND	High	High	Off (pull-down to GND)	Low
OFF Mode	Off	Off (ON @ V_{VS} > 2.0V)	High ohmic	High ohmic	Follows VIO (pull-up to VIO)	Follows VIO	Off (pull-down to GND)	Low

5.1.1 OFF Mode

This is the default mode when the battery is first connected. ATA650X is in OFF mode when the supply voltage of the device (V_{VS}) drops below the defined power-off detection voltage threshold ($V_{VS\_PWR\_OFF}$), or is below the power-on detection voltage threshold ($V_{VS\_PWR\_ON}$) during the supply voltage ramp up. In OFF mode, the IC is not able to provide any functionality. At V_{VS}>2V the voltage regulator is switched on. As soon as V_{VS} rises above the power-on detection threshold ($V_{VS\_PWR\_ON}$), the device transitions to Reset mode. The whole IC is reset, initialized, and switched into Reset mode.

5.1.2 Reset Mode

The ATA650X enters Reset mode:

- On initial power-up
- When an undervoltage event on VCC or VS occurs
- After a lifted VCC overtemperature event occurs
- After a wake-up event from Sleep mode occurs

During Reset mode, the communication is OFF, NRES is LOW, VCC is ON and the INH is ON.

When the supply voltage ramps up and the VS, VCC and VIO voltages are all above their corresponding thresholds, the device transitions to Standby mode after the t_{Reset} time has elapsed.

If the voltage on pin VIO is below V_{VIO_UV} for longer than $t_{VIO\_UV\_set}$, the device enters Sleep mode to save power.

5.1.3 Normal Mode

In Normal mode, the transceiver can transmit and receive data through the bus lines CANH and CANL. This is the normal transmitting and receiving mode of the CAN Interface, in accordance with the CAN specification. The output driver stage is active and drives data from the TXD input to the CAN bus. The High-Speed Comparator (HSC) converts the differential signal on the bus lines into a digital signal, which is output to the RXD pin. The bus biasing is set to $V_{VCC/2}$. The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible Electromagnetic Emission (EME).

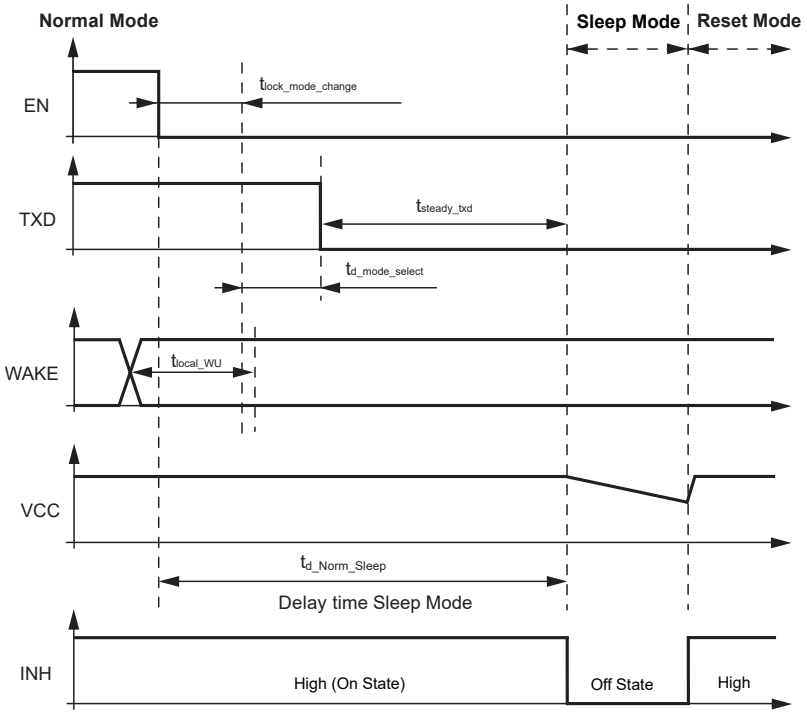
The VCC voltage regulator provides 5V at its output, with a low tolerance of ± 2% and a maximum output current of 150 mA. If a VCC undervoltage condition occurs, the NRES pin switches to low and the IC changes its state to Reset mode.

The INH output is switched ON, so external loads controlled by the INH pin are also switched ON.

In Normal mode, the wake-up source signalling at the TXD and RXD pins is deactivated.

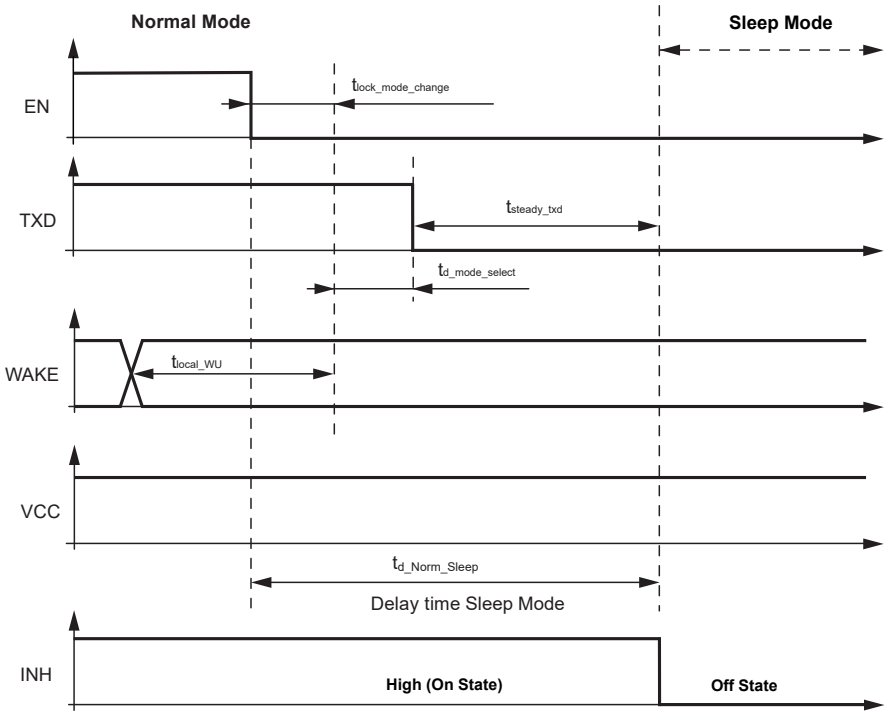
If a falling or rising edge at pin WAKE occurs shortly before a falling edge at pin EN, and the t_{local_WU} elapses after $t_{lock\_mode\_change}$, the local wake-up request will be stored. After entering Sleep mode, the device will automatically switch into Reset mode (see Figure 5-2).

Figure 5-2. Local wake-up request while switching from Normal mode to Sleep mode



If a falling or rising edge at pin WAKE occurs shortly before a falling edge at pin EN, but the t_{local_WU} elapses before $t_{lock\_mode\_change}$, the local wake-up request will be ignored and the device will enter Sleep mode (see Figure 5-3) and remain there.

Figure 5-3. Too early local wake-up request while switching from Normal mode to Sleep mode



5.1.4 Receive Only Mode

The Receive Only mode can be used to test the connection of the bus medium or to prevent a faulty CAN controller from disrupting network communication. In Receive Only mode, the ATA650X can still receive data from the bus, but the transmitter is disabled and therefore no data can be sent to the CAN bus. The bus pins are biased to a recessive state ($V_{VCC/2}$). All other IC functions, including the HSC, continue to operate as they do in Normal mode. The VCC Voltage regulator and the INH output operate in the same way as in Normal mode.

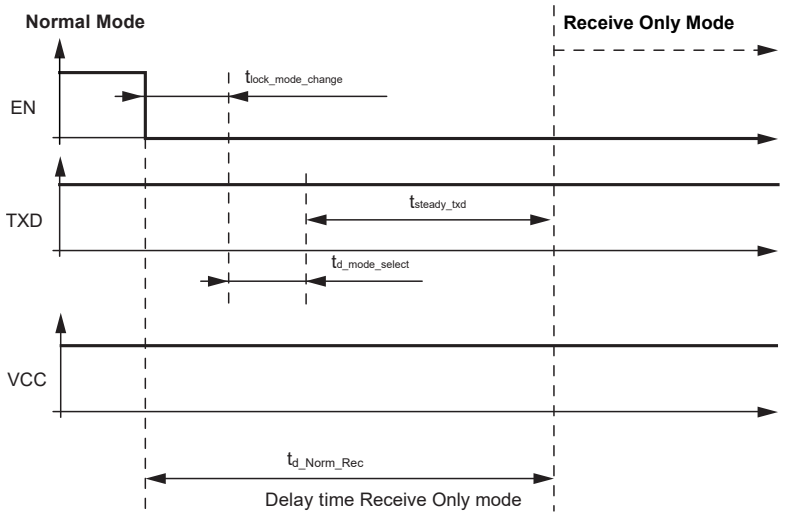
If a VCC undervoltage condition occurs during Receive Only mode, NRES is switched to low and the device transitions to Reset mode.

If V_{VIO} drops below its undervoltage detection threshold (V_{VIO_UV}), the transceiver switches OFF and disengages from the bus. The low-power Wake-Up Comparator is switched ON. If the voltage on pin VIO remains below V_{VIO_UV} for longer than $t_{VIO\_UV\_set}$, the device enters Sleep mode to save power and to ensure the bus is not disturbed.

If a CAN transceiver overtemperature occurs, the device switches from Normal into Receive Only mode and the transmitter is disabled. When the junction temperature drops below T_{Jsd}, and after a hysteresis of T_{JSD_hys}, the device switches again into Normal mode if EN and TXD pins are at high level.

A falling edge at EN, while TXD is high and held for $t_{d\_Norm\_Rec}$, switches the IC into Receive Only mode (only from Normal mode, see Figure 5-1). The TXD signal must be logic high during the mode select window, see figure below (Figure 5-4). The device can be set again into Normal mode with a high level at the EN pin, while TXD is high and the junction temperature is below T_{Jsd}.

Figure 5-4. Switching from Normal mode to Receive Only mode



5.1.5 Standby Mode

The Standby mode is the first level of power-saving mode for the ATA650X, offering reduced current consumption. In this mode, the transceiver is not able to transmit or correctly receive data through the bus lines. The transmitter and the HSC are switched OFF to reduce current consumption and only the low-power Wake-Up Comparator (WUC) monitors the bus lines for a valid wake-up signal.

The CAN transceiver in the ATA650X supports the autonomous bus biasing according to ISO 11898-2 in Standby mode (provided $V_{VCC} = V_{VCCnom}$). The bus pins are biased to GND (via R_{CAN_H}, R_{CAN_L}) when the bus is inactive for $t > t_{Silence}$ and to VCC/2 (at approximately 2.5V) when a remote CAN bus wake-up request (Wake-Up Pattern, WUP, according to ISO 11898-2) is detected.

Pin INH is still active, so external loads controlled by this pin are also active.

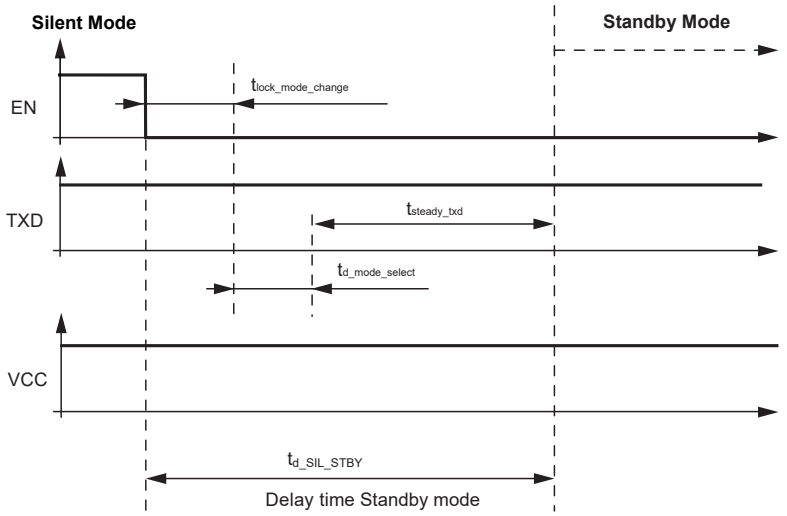
During Standby mode, the TXD pin is an output, and together with the RXD output pin signals the wake-up source, or a VS undervoltage. The signalling is prioritized: VS undervoltage has the highest priority, followed by the local wake-up, bus wake-up has the lowest priority.

The signalling is immediately deactivated if the Standby mode has been exited.

A high level at the EN pin, while TXD is high, will switch the device into Normal mode.

If the device is in Silent mode, a falling edge at the EN pin, while TXD is set to high, switches the IC into Standby mode. The TXD pin must be logic high during the mode select window (t_{steady_txd}), see figure below (Figure 5-5).

Figure 5-5. Switching from Silent mode to Standby mode



5.1.6 Silent Mode

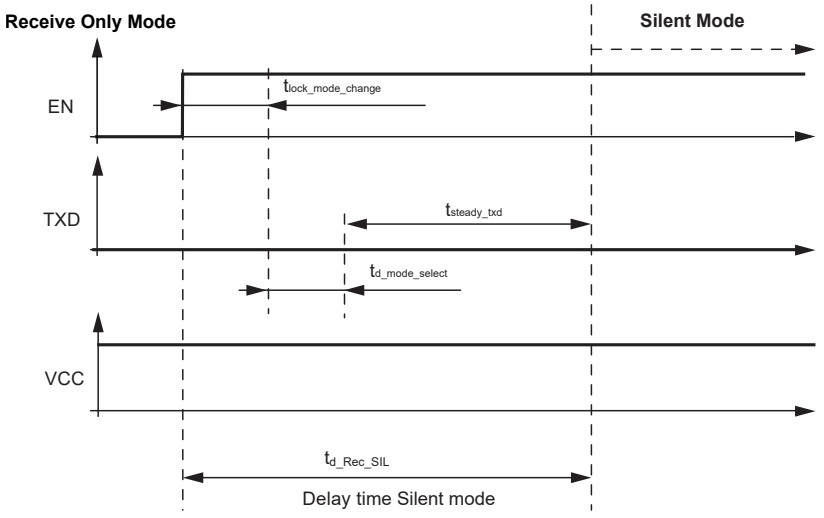
The Silent mode is a power-saving mode of the ATA650X, offering reduced current consumption. In this mode, the VCC voltage regulator is switched ON but the transceiver is not able to transmit or receive data through the bus lines. The wake-up signaling is deactivated, , which means in Silent Mode the ARTA650x cannot be woken up via the bus lines and also not via the WAKE pin.

The CAN transceiver in the ATA650X supports the autonomous bus biasing according to ISO 11898-2 in Silent mode (provided $V_{VCC} = V_{VCCnom}$). The bus pins are biased to GND (via R_{CAN_H}, R_{CAN_L}) when the bus is inactive for $t > t_{Silence}$ and to VCC/2 (at approximately 2.5V) when a remote CAN bus wake-up request (Wake-Up Pattern, WUP, according to ISO 11898-2) is detected.

Pin INH output is still switched ON, so the external loads controlled by this pin are also powered.

A rising edge at EN pin, while TXD is set to low, switches the IC into Silent mode (only from Receive Only mode). The TXD signal must be logic low during the mode select window (t_{steady_txd}), see figure below (Figure 5-6).

Figure 5-6. Switching from Receive Only mode to Silent mode

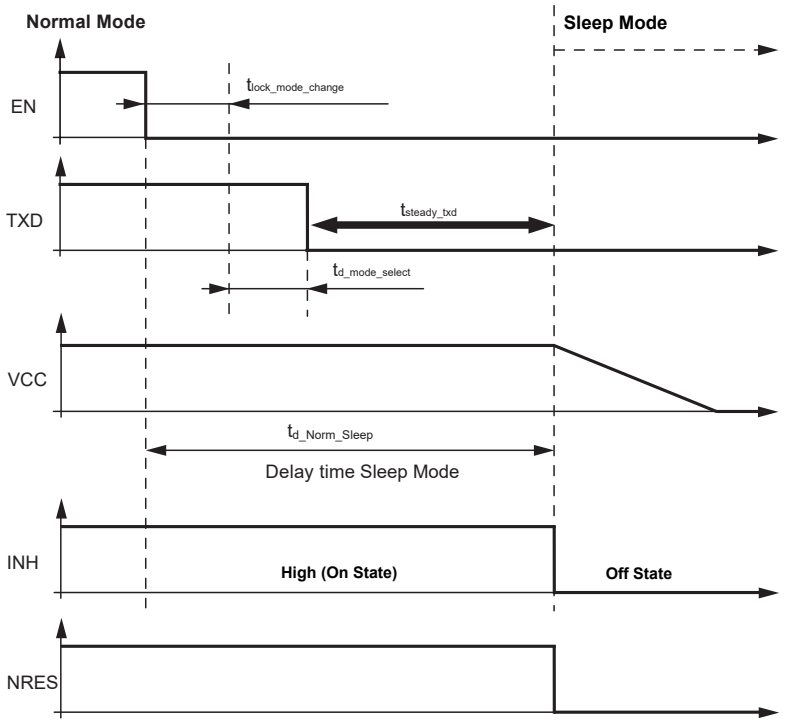


5.1.7 Sleep Mode

The Sleep mode is the highest power-saving mode of the device. In this mode, the internal VCC voltage regulator is switched OFF. The INH output is also switched OFF and therefore the external circuitry connected to this pin is also switched OFF.

A falling edge at EN while TXD is low switches the IC into Sleep mode. The TXD signal must be logic low during the mode select window, see figure below (Figure 5-7). In this mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transceiver is disabled, except for a low-power Wake-Up Comparator (WUC).

Figure 5-7. Switching to Sleep mode



To avoid any influence on the CAN pins when switching into Sleep mode, the EN pin should be set to LOW first, and after the time $t_{lock\_mode\_change}$ where the TXD pin should stay HIGH, the TXD pin can be set to LOW, but not later than the $t_{d\_mode\_select}$ time has elapsed.

In Sleep mode, the bus lines are biased to ground to reduce current consumption to a minimum.

5.1.7.1 Remote Wake-Up through the CAN Bus

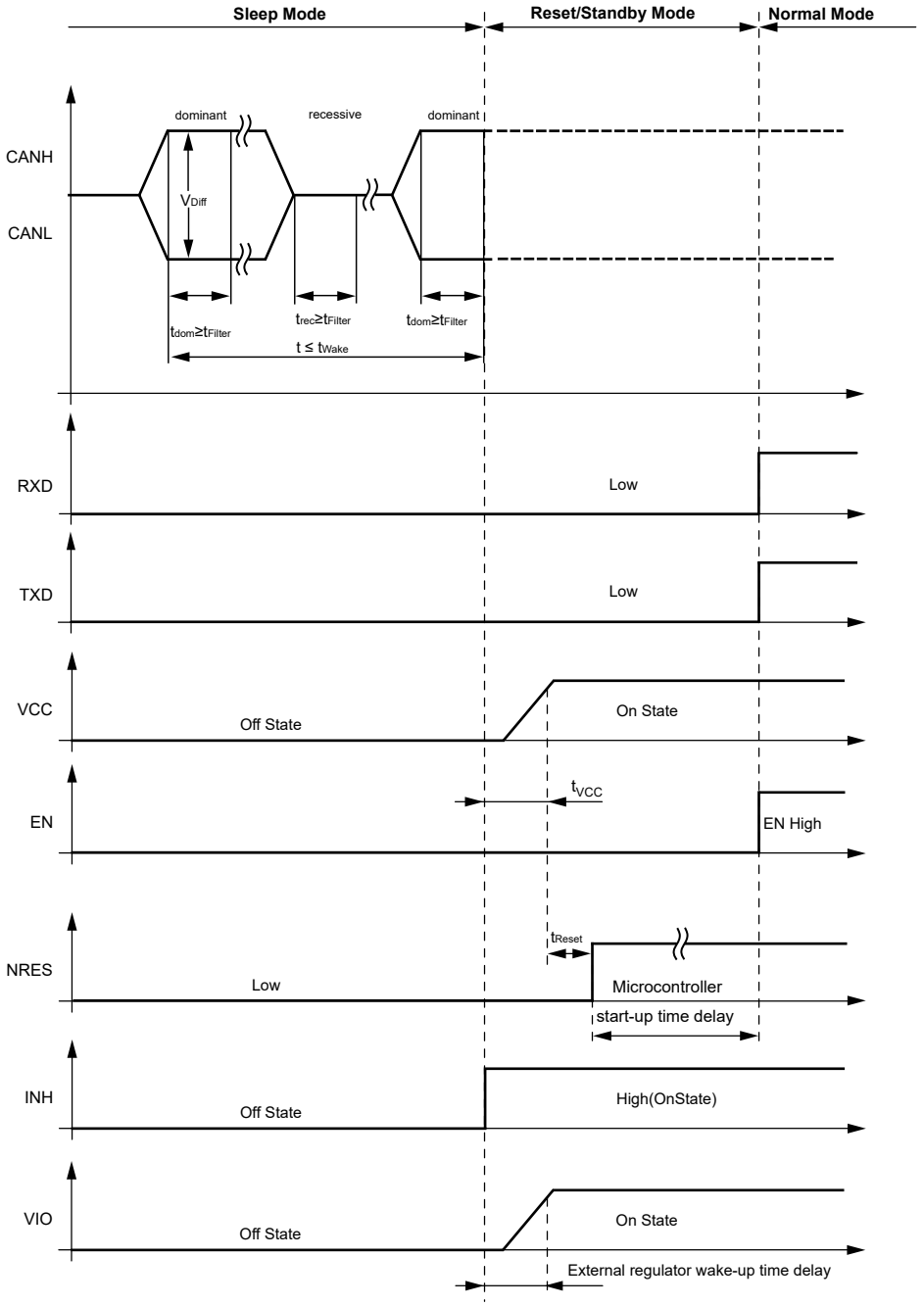
The ATA650X monitors the bus lines for a valid WUP, as specified in the ISO 11898-2:2024. This filtering helps to avoid spurious wake-up events, which can be triggered by scenarios such as a dominant clamped bus, a dominant phase due to noise, spikes on the bus, transients or EMI.

The Wake-Up Pattern consists of at least two consecutive dominant bus levels for a duration of at least t_{Filter}, each separated by a recessive bus level with a duration of at least t_{Filter}. Dominant or recessive bus levels shorter than t_{Filter} are always ignored. The complete dominant-recessive-dominant pattern must be received within the bus wake-up time-out time t_{wake}, to be recognized as a valid Wake-Up Pattern, as shown in Figure 5-8. Otherwise, the internal wake-up logic is reset and then the complete Wake-Up Pattern must be detected to trigger a wake-up event.

During Normal mode, at VCC or VIO undervoltage conditions, or when the complete Wake-Up Pattern is not received within t_{wake}, no wake-up is signalled at the RXD pin and the TXD pin.

When a valid Wake-Up Pattern is received, the device enters Reset mode; the voltage regulator and the INH output are switched ON.

Figure 5-8. CAN Bus Wake-Up Timing



When a valid CAN WUP is detected on the bus, the RXD pin and TXD pin switch to low to signal a CAN bus wake-up request.

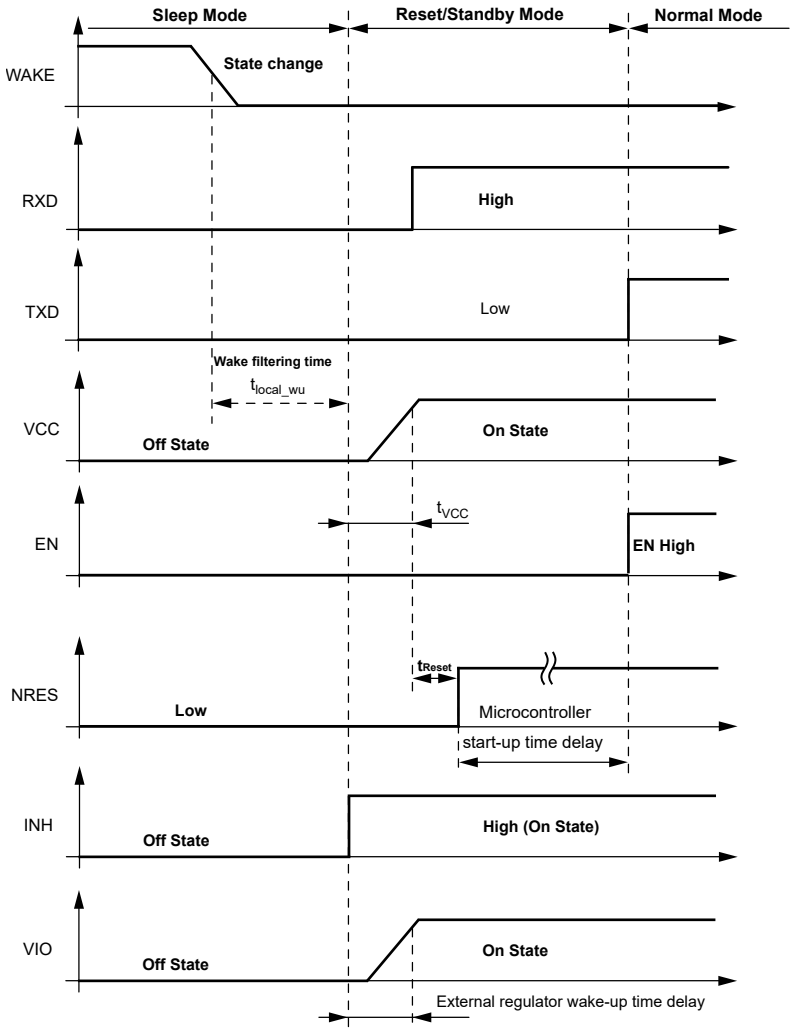
5.1.7.2 Local Wake-Up via the WAKE Pin

A falling or rising edge at the WAKE pin, followed by a low or high level maintained for a given time period (> t_{local_wu}), results in a local wake-up request. The device switches to Reset mode and then to Standby mode.

The Autonomous bus biasing is active. The local wake-up request is signalled to the microcontroller by a high level at the RXD pin and a low level at the TXD pin.

The VCC output voltage reaches 4V after t_{VCC}. Note that the time (t_{VCC}) required for VCC to reach 4V depends on the externally applied VCC capacitor and the connected load. The NRES output remains low for the reset time delay t_{Reset}. The behavior of a local wake-up is shown in Figure 5-9.

Figure 5-9. Local Wake-Up via the WAKE Pin from Sleep mode



5.2 Fail-Safe Features

The ATA650X can detect a number of different local failure conditions, which are described in the following chapters.

5.2.1 TXD Dominant Time-Out Function

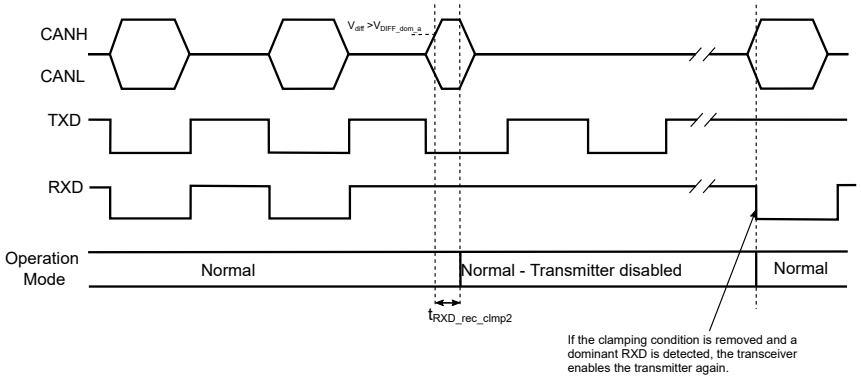
A permanent low level on pin TXD (due to a hardware or software application failure) would drive the CAN bus into a permanent dominant state, blocking all network communication. The TXD dominant time-out function prevents such a network lock-up by disabling the transmitter. The TXD dominant time-out timer is started when the TXD pin is set to low. If the low state on the TXD pin persists for longer than $t_{to(dom)}$, the transmitter is disabled, releasing the bus lines to a recessive state. The $t_{to(dom)}$ dominant time-out timer defines the minimum possible bit rate. In order to reset the TXD dominant time-out timer, the TXD pin must be set to high for longer than $t_{TX\_resume\_TXDOUT}$.

5.2.2 RXD Recessive Clamping

This fail-safe feature prevents the controller from sending data to the bus if its RXD line is clamped to high (recessive). If the RXD pin cannot signal a dominant bus state because it is shorted to

VCC, the transmitter within the ATA650X is disabled to avoid possible data collisions on the bus. In Normal mode, the device continuously compares the state of the the high-speed comparator (HSC) with the state of the RXD pin. If the HSC indicates a dominant bus state for more than $t_{RXD\_rec\_clmp}$, without the RXD pin indicating the same, a recessive clamping failure is detected. The RXD recessive clamping detection is reset by either entering Sleep or OFF mode or if the RXD pin shows a dominant (LOW) level again.

Figure 5-10. RXD Recessive Clamping Detection



5.2.3 Behaviour Under Low Supply Voltage

After the battery voltage has been connected to the application circuit, the voltage at the VS pin increases according to the bypass capacitor used in the application (see Typical Application Circuit). If V_{VS} is higher than the threshold for power-on detection ($V_{VS\_PWR\_ON}$), the IC mode changes from OFF mode to Reset mode, and if the output voltage of VCC rises above the undervoltage threshold ($V_{VCC\_th\_UV\_UP}$) for longer than the Reset time (t_{Reset}), the device automatically enters Standby mode. Note that t_{Reset} starts when the rising VCC voltage reaches the VCC undervoltage clear threshold $V_{VCC\_th\_UV\_UP}$. As soon as V_{VS} exceeds the undervoltage threshold $V_{VS\_th\_UV\_UP}$, the CAN transceiver can be activated.

The VCC output voltage reaches 4V after t_{VCC}. The time t_{VCC} depends on the externally applied VCC capacitor and the connected load. The NRES output is low for the reset time delay t_{Reset}. The behavior of VCC, the NRES, and VS is shown in Figure 5-11 and Figure 5-12.

Figure 5-11. VCC and NRES versus VS (Ramp-up)

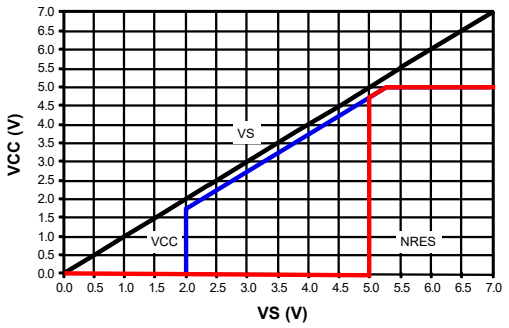
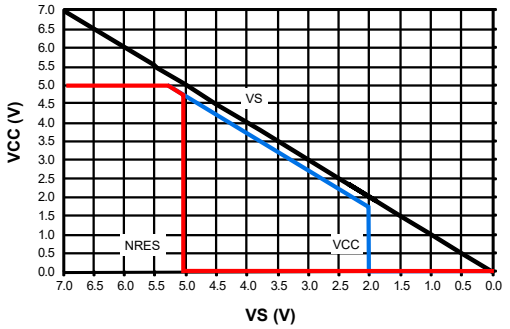


Figure 5-12. VCC and NRES versus VS (Ramp-Down)



The graphs are only valid if the VS ramp-up and ramp-down times are much slower than the VCC ramp-up time t_{VCC} and the reset NRES delay time t_{Reset}. If, during Sleep mode, the voltage level of V_{VS} drops below the undervoltage detection threshold $V_{VS\_th\_UV\_DOWN}$, the operation mode is not changed and no wake-up is possible. Only if the supply voltage on pin VS drops below the VS operation threshold $V_{VS\_PWR\_OFF}$, the IC switches to OFF mode. If, during Receive Only mode, the VCC voltage drops below the VCC undervoltage threshold $V_{VCC\_th\_UV\_DOWN}$, the IC switches into Reset mode. If the supply voltage on pin VS drops below the threshold for power-off detection $V_{VS\_PWR\_OFF}$, the IC switches to OFF mode. If, during Normal mode, the voltage level on the VS pin drops below the VS undervoltage detection threshold $V_{VS\_th\_UV\_DOWN}$, the IC switches to Reset mode. This means the CAN transceiver is disabled to avoid malfunctions or corrupted bus messages. The voltage regulator remains active.

During a VCC undervoltage situation, the IC is in Reset mode and can only be switched into Sleep mode. Only when the supply voltage V_{VS} drops below the power-off threshold $V_{VS\_PWR\_OFF}$ does the IC switch into OFF mode.

If V_{VIO} drops below its undervoltage detection threshold (V_{VIO_UV}), the transceiver switches OFF and disengages from the bus. The low-power Wake-Up Comparator is switched ON. If the voltage on pin VIO remains below V_{VIO_UV} for longer than $t_{VIO\_UV\_set}$, the device enters Sleep mode to save power and to ensure the bus is not disturbed.

A VIO undervoltage event is not signalled on NRES.

5.2.4 Bus Wake-Up only at Dedicated Wake-Up Pattern

Due to the implementation of the wake-up filtering, the ATA650X does not wake up when the bus is in a long dominant state; it only wakes up when a valid Wake-Up Pattern (WUP) specified in the ISO 11898-2:2024 has been detected. For a valid wake-up, at least two consecutive dominant bus levels for a duration of at least t_{Filter}, each separated by a recessive bus level with a duration of at least t_{Filter}, must be received from the bus. Dominant or recessive bus levels shorter than t_{Filter} are always ignored. The complete dominant-recessive-dominant pattern (as shown in Figure 5-8) must be received within the bus wake-up time-out time t_{wake} to be recognized as a valid WUP. This filtering significantly reduces unwanted bus wake-up due to noise.

5.2.5 Overtemperature Detection of the VCC Voltage Regulator

The VCC voltage regulator is protected against overtemperature.

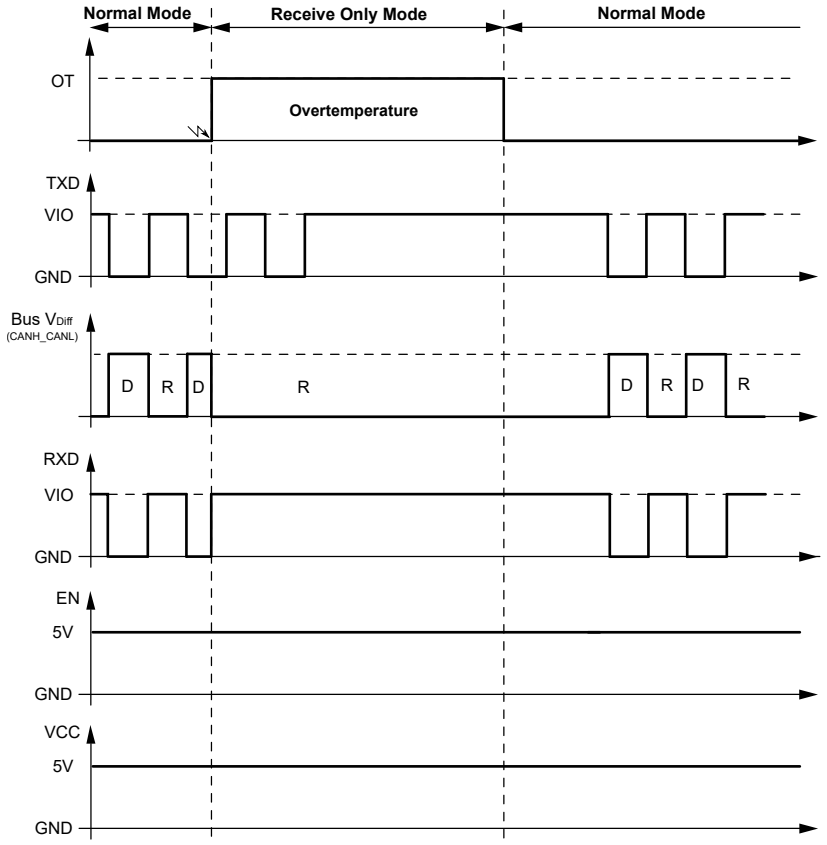
If the junction temperature exceeds the shutdown junction temperature, T_{Jsd}, the device switches into VCC Overtemp mode, where the VCC output, the communication and the INH output are switched OFF. Once the junction temperature drops below T_{Jsd}, minus a hysteresis of T_{Jsd_hys}, the device switches into Reset mode and switches ON the VCC voltage regulator and the INH output again.

During overtemperature, the NRES pin is asserted to low.

5.2.6 Overtemperature Detection of the CAN Transceiver

The CAN transceiver is protected against overtemperature conditions. In Normal mode, if the junction temperature exceeds the shutdown junction temperature, T_{Jsd}, the device switches into Receive Only mode and the transmitter is disabled. When the junction temperature drops below T_{Jsd}, the device switches again into Normal mode when EN and TXD pins are at high level, as shown in Figure 5-13.

Figure 5-13. Release of Transmission after CAN Transceiver Overtemperature Condition



5.2.7 Overvoltage Protection

The VCC voltage regulator is protected against overvoltage conditions. In case of an overvoltage at VCC, the voltage regulator will be switched OFF and the device switches into Sleep mode.

When the device is in Normal mode and an overvoltage at VCC occurs, the device switches immediately into Sleep mode. Leaving Sleep mode after an overtemperature event is possible either with a wake-up via the CAN bus or WAKE pin, or a rising edge at the EN pin.

5.2.8 Short Circuit Protection of the Bus Pins

The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage. A current-limiting circuit protects the transceiver against damage. If the device is heating up due to a continuous short on CANH or CANL, the internal overtemperature protection switches OFF the bus transmitter.

5.2.9 Internal Pull Up and Pull Down Structures

The TXD pin has an internal pull-up resistor to VIO. This ensures a safe and defined state in case the pin is left floating.

The EN pin has an internal pull-down resistor to force the device into recessive mode if EN is disconnected.

The INH pin has an internal pull-down resistor, which is activated when the INH output switch is turned OFF. This ensures a defined level at the INH pin, when the output is switched OFF.

5.3 Wake-Up Source/ VS Undervoltage Signalling

The device can distinguish between different wake-up sources. The wake-up source can be read on the TXD and RXD pins in Standby mode. These flags are immediately reset if the ATA650X has exited Standby mode. The signalling in Standby mode is shown in Table Table 5-2.

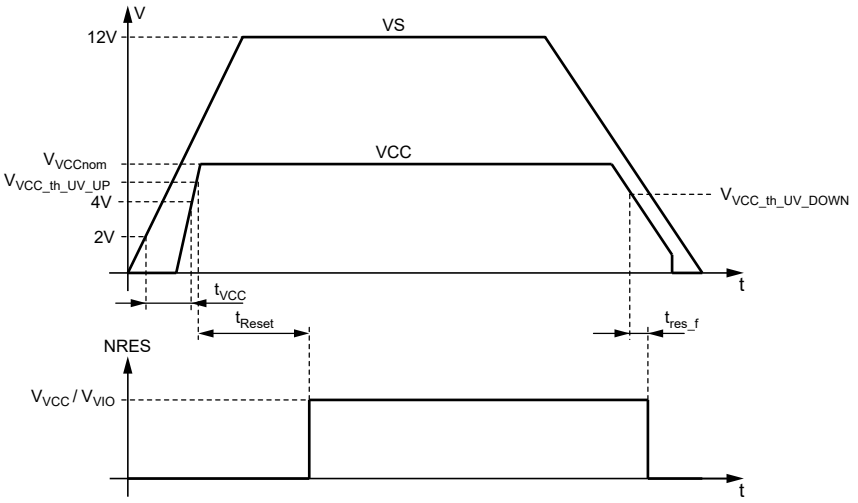
Table 5-2. Signalling in Standby mode

Wake-up Source / VS Undervoltage Signalling	TXD	RXD
CAN bus wake-up	Low	Low
Local wake-up (WAKE pin)	Low	High
VS undervoltage detection ($V_{VS} < V_{VS\_th\_UV\_DOWN}$)	High	Low

5.4 Internal Voltage Regulator

The internal 5V VCC voltage regulator is capable of driving loads up to 150 mA, supplying the microcontroller and other devices on the PCB, and is protected against overload by means of current limitation and overtemperature shutdown. Furthermore, the output voltage is monitored and causes a reset signal NRES if it drops below a defined threshold $V_{VCC\_th\_uv\_down}$.

Figure 5-14. VCC Low Drop Voltage Regulator: Supply Voltage Ramp-up and Ramp-Down



The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommended to use an MLC capacitor with a minimum capacitance of 2.2 µF together with a 100 nF ceramic capacitor. The values of these capacitors must be adjusted to the needs of the application.

During a short circuit at VCC, the output limits the output current to I_{VCClim}; due to the undervoltage in this situation, the NRES output switches to low. If the chip temperature exceeds the value T_{Jsd}, the VCC output switches OFF. The chip cools down and, after a hysteresis of T_{Jsd_hys}, the output switches ON again. When the ATA650X is being soldered onto the PCB, it is mandatory to connect the exposed thermal pad with a wide GND plate on the printed board to create a good heat sink. The main power dissipation of the IC is created from the VCC output current I_{VCC}, which is needed for the application.

The internal CAN transceiver typically consumes 50 mA while driving a dominant bus state, leaving 100 mA available for the external load on pin VCC. The average current consumption of the CAN

transceiver is lower (≈ 25 mA), depending on the application, leaving more current available for the load.

Figure 5-15. VDFN8 Package - Power Dissipation and Safe Operating Area: ATA6500 and ATA6501 voltage regulator's output current I_{VCC} versus supply voltage V_{VS} at different ambient temperatures (R_{thjA} = 53K/W)

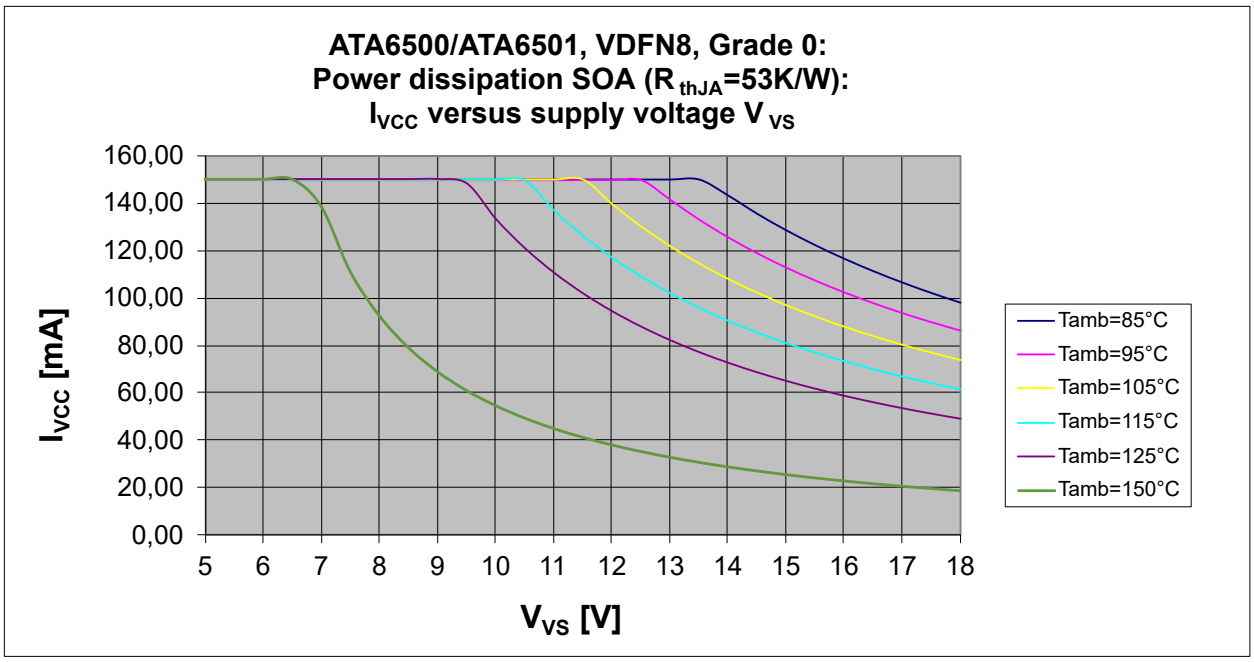


Figure 5-16. VDFN10 Package - Power Dissipation and Safe Operating Area: ATA6502 and ATA6503 voltage regulator's output current I_{VCC} versus supply voltage V_{VS} at different ambient temperatures (R_{thjA} = 50K/W)

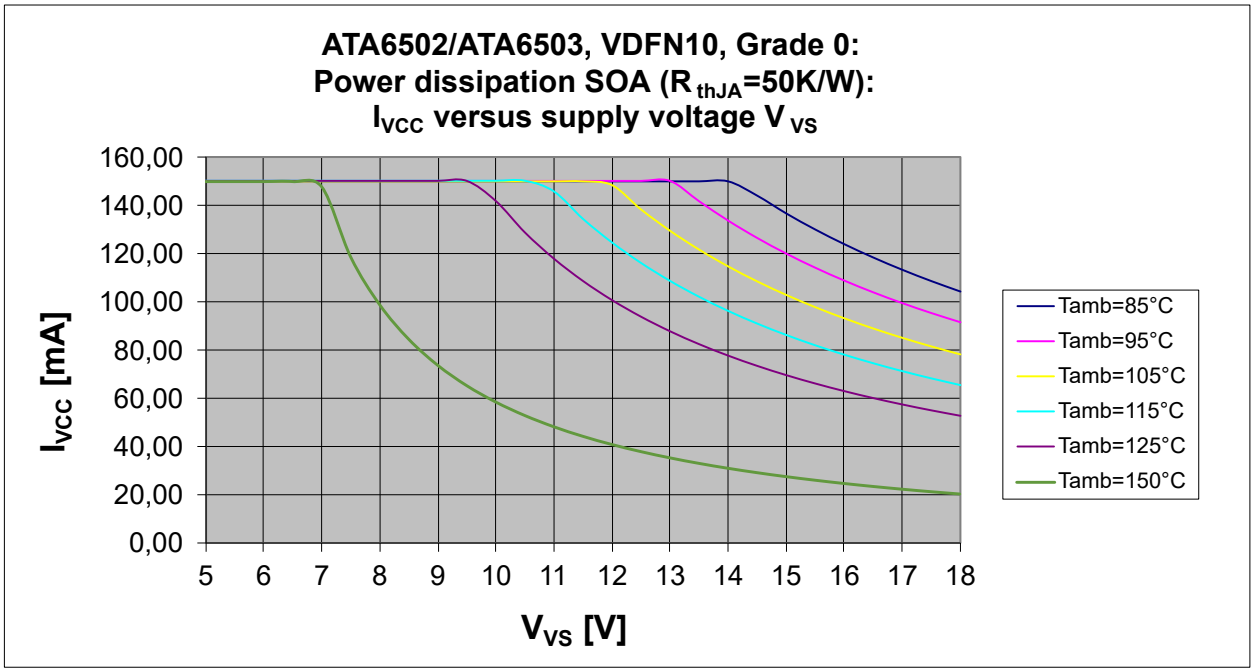
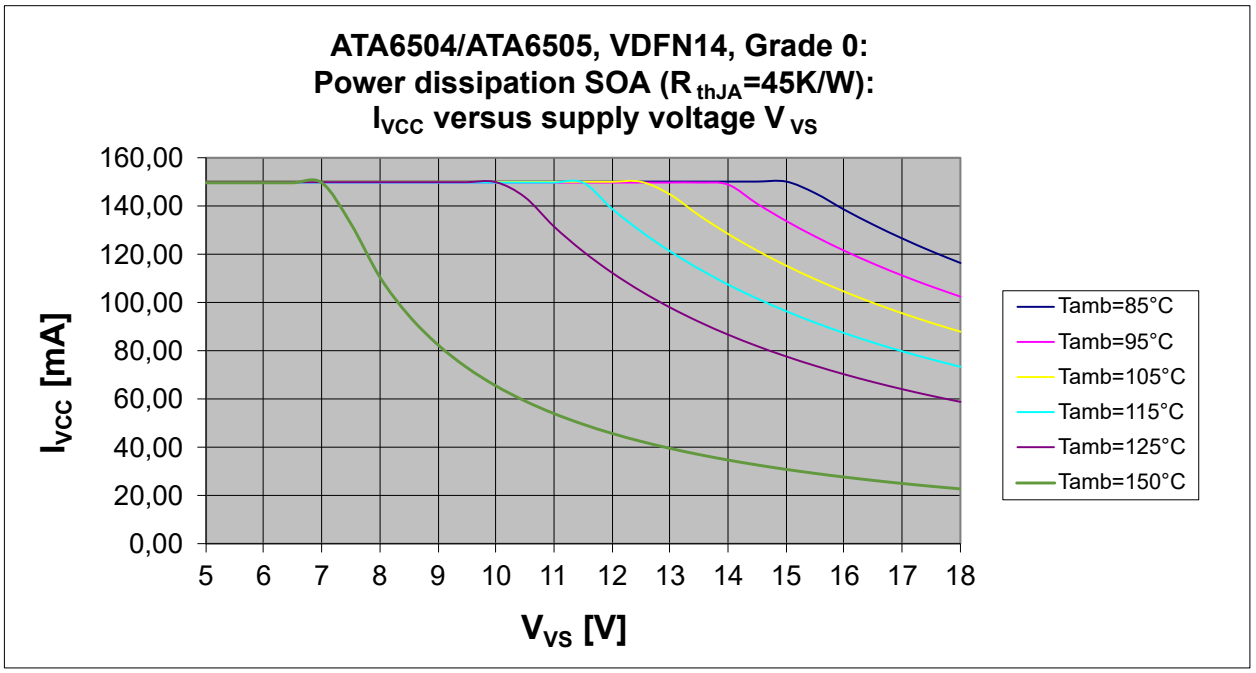


Figure 5-17. VDFN14 Package - Power Dissipation and Safe Operating Area: ATA6504 and ATA6505 voltage regulator's output current I_{VCC} versus supply voltage V_{VS} at different ambient temperatures (R_{thjA} = 45K/W)



6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Sym.	Min.	Max.	Unit
DC Voltage on Pin VS	V_{VS}	–0.3	+40	V
DC Voltage on Pin WAKE	V_{WAKE}	–1.2	+40	V
DC Voltage on Pin INH	V_{INH}	–0.3	V_{VS}+0.3V	V
DC Current on Pin INH	I_{INH}	–	-20	mA
DC Voltage on Pins CANH, CANL	V_{CANH}, V_{CANL}	–27	+42	V
Transient Voltage, according to ISO 7637 part 3		–150	+100	V
Maximum Differential Bus Voltage	V_{Diff}	–40	+40	V
DC Voltage on Pins VCC, VIO, EN, NRES	V_x	–0.3	+5.5	V
DC Voltage on Pins TXD, RXD	V_x	–0.3	V_{VIO}+0.3	V
DC Output Current on Pin VCC	I_{VCC}	–	-150	mA
DC Input Current on Pin VCC	I_{VCC}	–	+200	mA
ESD according to IBEE CAN EMC Test Specification following IEC 62228, IEC 61000-4-2 (330Ω/150 pF): Pins VS, CANH, CANL, WAKE to GND	—	+/–6	—	kV
HBM JESD22-A114/AEC-Q100-002 (1.5 kΩ/100 pF): • CANH, CANL, VS, WAKE to GND	—	+/–8	—	kV
HBM JESD22-A114/AEC-Q100-002 (1.5 kΩ/100 pF): All Pins	—	+/–6	—	kV
Charge Device Model ESD AEC-Q100-011	—	+/–750	—	V
Machine Model ESD AEC-Q100-003	—	+/–200	—	V
Storage Temperature	T_{stg}	–55	+150	°C
Virtual Junction Temperature	T_{vJ}	–40	+175	°C

6.2 DC/AC Characteristics

All parameters valid for T_{amb} = –40°C to +150°C; $T_{vj} \leq 170°C$; $3.1V \leq V_{VS} \leq 28V$; $4.5V \leq V_{VCC} \leq 5.5V$; $1.8V \leq V_{VIO} \leq 5.5V$; all voltages are defined with respect to ground; $R_{(CANH-CANL)} = 60\Omega$; C_L = 100 pF; typical values are given at V_{VS} = 13V, T_{amb} = +25°C; unless otherwise noted.

No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
VS									
0.01	Supply Voltage Threshold for Power-On Detection	V_{VS} rising	VS	$V_{VS\_PWR\_ON}$	4.1	—	4.55	V	B
0.02	Supply Voltage Threshold for Power-Off Detection	V_{VS} falling	VS	$V_{VS\_PWR\_OFF}$	2.8	—	3.1	V	A
0.03	Supply Voltage Threshold for CAN TRX Undervoltage Detection Release	V_{VS} rising	VS	$V_{VS\_th\_UV\_UP}$	4.5	—	4.9	V	A
0.04	Supply Voltage Threshold for CAN TRX Undervoltage Detection Set	V_{VS} falling	VS	$V_{VS\_th\_UV\_DOWN}$	4.2	—	4.55	V	A
0.051	VS Supply Current	Sleep mode; $7 < V_{VS} < 18V$, $T_{amb} \leq 65°C$	VS	I_{VS_SLP}	—	15	20	µA	B
0.052		Sleep mode; $7 < V_{VS} < 18V$, $T_{amb} \leq 150°C$	VS	I_{VS_SLP}	—	—	30	µA	A
0.053		Standby /Silent mode; $7 < V_{VS} < 18V$, $T_{amb} \leq 65°C$	VS	I_{VS_STB}	—	—	45	µA	B
0.054		Standby/Silent mode; $7 < V_{VS} < 18V$, $T_{amb} \leq 150°C$	VS	I_{VS_STB}	—	—	60	µA	A
0.055		Additional current in Standby/Silent mode, when the auto biasing is active; $7 < V_{VS} < 18V$, $T_{amb} \leq 65°C$	VS	$I_{VS\_STB\_autobias}$	—	—	150	µA	B
0.056		Additional current in Standby/Silent mode, when the auto biasing is active; $7 < V_{VS} < 18V$, $T_{amb} \leq 150°C$	VS	$I_{VS\_STB\_autobias}$	—	—	160	µA	A
0.057		Receive Only mode; $7 < V_{VS} < 18V$	VS	$I_{VS\_Receive\_Only}$	—	—	350	µA	A

.....continued

No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
0.058	VS Supply Current	Normal mode; $7 < V_{VS} < 18V$	VS	$I_{VS\_N\_Rec}$	—	—	5	mA	A
0.059		Normal mode; $7 < V_{VS} < 18V$	VS	$I_{VS\_N\_Dom}$	—	—	75	mA	A
0.060		Normal mode; $7 < V_{VS} < 18V$, short between CANH and CANL	VS	$I_{VS\_CAN\_short}$	—	—	80	mA	B
VCC									
1.01	Output Voltage	$V_{VS} > 5.8V$ I_{VCC} = 0 to -85 mA	VCC	V_{VCCnom}	4.9	-	5.1	V	A
1.011	Output Voltage	$V_{VS} > 5.8V$ I_{VCC} = 0 to -150 mA	VCC	V_{VCCnom}	4.9	-	5.1	V	C
1.02	Load Step Response	$V_{VS} > 5.8V$ C_{VCC} = 4.7 µF I_{VCC} = 0 to -150 mA	VCC	$V_{VCC\_LoadStep}$	-2	-	+2	%	C
1.03	Output Voltage at low VS	$4V < V_{VS} < 5.75V$ (I_{VCC} = 0 to -150 mA)	VCC	V_{VCClow}	V_{VS}-V_D	-	5.1	V	A
1.041	Regulator Drop Voltage	$V_{VS} > 4V$, I_{VCC} = -20 mA	VCC	V_{D1}	-	-	100	mV	A
1.042		$V_{VS} > 4V$, I_{VCC} = -50 mA	VCC	V_{D2}	-	-	250	mV	A
1.043		$V_{VS} > 4V$, I_{VCC} = -150 mA	VCC	V_{D3}	-	-	750	mV	A
1.05	Line Regulation	$5.75V < V_{VS} < 28V$ I_{VCC} = 20 mA	VCC	$V_{VCCline}$	-	-	0.2	%	A
1.06	Load Regulation	V_{VS} = 12V -5 mA < I_{VCC} < -150 mA	VCC	$V_{VCCload}$	-	-	0.5	%	C
1.07	Output Current Limitation	V_{VS} = 5.75V	VCC	I_{VCClim}	-380		-200	mA	A
1.08	Load capacitance	MLC capacitor	VCC	C_{load}	1.87	2.2	-	µF	D
1.09	Ramp-up Time	$V_{VS} > 5.75V$, after enable VCC regulator to V_{VCC} = 4V, C_{VCC} = 4.7 µF, R_{load} = 1 kOhm at VCC	VCC	t_{VCC}	-	-	0.5	ms	B
1.1	VCC Undervoltage Set Threshold	V_{VCC} falling	VCC	$V_{VCC\_th\_UV\_DOWN}$	4.55	-	4.75	V	A
1.11	VCC Undervoltage Clear Threshold	V_{VCC} rising	VCC	$V_{VCC\_th\_UV\_UP}$	4.65	-	4.85	V	A
1.12	VCC Undervoltage Hysteresis		VCC	$V_{UV\_VCC\_HYS}$	0.08	0.1	0.12	V	C
1.13	VCC Undervoltage Detection Set Time		VCC	$t_{VCC\_UV\_falling}$	6	—	54	µs	A
1.14	VCC Undervoltage Detection Recover Time		VCC	$t_{VCC\_UV\_rising}$	6	—	54	µs	A
1.15	VCC Pull Down Resistor while VCC is OFF	Sleep mode	VCC	$R_{VCC\_PULL\_DOWN}$		15		kΩ	A

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No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
1.16	VCC Overvoltage Set Detection Threshold	V_{VCC} rising	VCC	$V_{VCC\_OV\_Set}$	5.25	-	5.5	V	A
1.17	VCC Overvoltage Clear Detection Threshold	V_{VCC} falling	VCC	$V_{VCC\_OV\_Clear}$	5.20	-	5.45	V	A
1.18	VCC Overvoltage Hysteresis		VCC	$V_{VCC\_OV\_hys}$	0.03	0.05	0.07	V	C
1.19	VCC Overvoltage Detection Set Time		VCC	$t_{VCC\_OV\_falling}$	6	—	54	µs	A
VIO									
2.01	Supply Voltage on Pin VIO		VIO	V_{VIO}	1.65	—	5.5	V	A
2.02	Supply Current on Pin VIO	Normal and Receive Only mode. Recessive, $V_{TXD} = V_{VIO}$	VIO	I_{VIO_Rec}	—	—	1.0	µA	A
2.03		Normal and Receive Only mode. Dominant, V_{TXD} = 0V, V_{VIO} = 5V, R_{TXD} = 40 kΩ	VIO	I_{VIO_Dom}	—	—	140	µA	A
2.04		Standby / Sleep mode	VIO	$I_{VIO\_STB\_SLP}$	—	—	1.0	µA	A
2.05	VIO Undervoltage Detection Threshold (1.8V and 5V)	ATA6500 ATA6502 ATA6504	VIO	V_{VIO_UV}	1.45	—	1.65	V	A
2.06	VIO Undervoltage Detection Threshold (3.3V and 5V)	ATA6501 ATA6503 ATA6505	VIO	V_{VIO_UV}	2.90	—	3.15	V	A
2.07	VIO Undervoltage Detection Threshold Hysteresis		VIO	$V_{UV\_VIO\_HYS}$	—	100	—	mV	A
2.08	VIO Undervoltage Detection Set Time		VIO	$t_{VIO\_UV\_falling}$	6	—	54	µs	A
2.09	VIO Undervoltage Detection Recover Time		VIO	$t_{VIO\_UV\_rising}$	6	—	54	µs	A
2.10	VIO Undervoltage Detection Time		VIO	$t_{VIO\_UV\_set}$	200	300	400	ms	A
EN									
3.01	High-Level Input Voltage		EN	V_{IH}	1.2	—	5.5	V	A
3.02	Low-Level Input Voltage		EN	V_{IL}	−0.1	—	0.9	V	A
3.03	Hysteresis		EN	V_{EN_hys}	50	—	100	mV	A
3.04	Pull-down Resistor	$V_{EN} = V_{VIO}$	EN	R_{EN}	50	125	200	kΩ	A
3.05	Low-Level Input Current	V_{EN} = 0V	EN	I_{EN}	−3.0	—	3.0	µA	A
NRES									
4.01	Low-Level Output Voltage	$V_{VS} \geq 5.5V$, I_{NRES} = 2 mA	NRES	V_{NRES}	—	0.2	0.4	V	A
4.02	Undervoltage Reset Time	$V_{VS} \geq 5.5V$, C_{NRES} = 20 pF	NRES	t_{Reset}	2	4	6	ms	A

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No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
4.03	Reset Debounce Time for Falling Edge	$V_{VS} \geq 5.5V$, $C_{NRES} = 20$ pF	NRES	t_{res_f}	6	—	54	µs	A
4.04	Switch-Off Leakage Current	$V_{NRES} = 5.5V$	NRES	I_{NRES_L}	-3	—	3	µA	A
WAKE									
5.01	High-Level Input Current	$V_{WAKE} = 4.2V$, $V_{VS} \geq 5.2V$	WAKE	I_{WAKE_H}	-10	-5	-1	µA	A
5.02	Low-Level Input Current	$V_{WAKE} = 2.3V$	WAKE	I_{WAKE_L}	1	5	10	µA	A
5.03	WAKE Threshold Voltage	WAKE rising, $V_{VS} \geq$ $V_{S\_th\_UV\_UP}$	WAKE	$V_{WAKE\_TH\_R}$	2.8	—	4.1	V	A
5.04	WAKE Threshold Voltage	WAKE falling, $V_{VS} \geq$ $V_{S\_th\_UV\_UP}$	WAKE	$V_{WAKE\_TH\_L}$	2.4	—	3.75	V	A
5.05	WAKE Input Hysteresis Voltage		WAKE	V_{WAKE_hys}	0.2	—	0.6	V	A
5.06	Debounce Time of Pulse for Wake-Up via WAKE pin	Falling/Rising Edge on Pin WAKE	WAKE	t_{local_wu}	50	100	150	µs	A
TXD									
6.01	High-Level Input Voltage		TXD	V_{TXD_H}	$0.7 \times V_{VIO}$	—	$V_{VIO} + 0.3$	V	A
6.02	Low-Level Input Voltage		TXD	V_{TXD_L}	−0.3	—	$0.3 \times V_{VIO}$	V	A
6.03	Pull-Up Resistor	$V_{TXD} = 0V$	TXD	R_{TXD}	40	55	90	kΩ	A
6.04	High-Level Leakage Current	Normal mode, $V_{TXD} = V_{VIO}$	TXD	I_{TXD}	-2	—	2	µA	D
6.05	Low-Level Output Sink Current at Wake-Up Request	Standby mode, $V_{TXD} = 0.4V$	TXD	I_{TXD}	1.5	2.5	8	mA	A
6.06	Input Capacitance		TXD	C_{TXD}	—	5	10	pF	D
RXD									
7.01	High-Level Output Current	Normal mode, Bus Recessive, $V_{RXD} = V_{VIO} - 0.4V$, $V_{VIO} = V_{VCC}$	RXD	I_{OH}	−8	—	-1.4	mA	A
7.02	Low-Level Output Current	Normal mode, $V_{RXD} = 0.4V$, Bus Dominant	RXD	I_{OL}	1.4	—	12	mA	A
INH									
11.01	High-Level Voltage	Normal mode, Standby mode, Receive Only or Reset mode, $I_{INH} = -2$ mA	INH	V_{INH_H}	$V_{VS} - 0.8$	—	V_{VS}	V	A
11.02	OFF mode Leakage Current	OFF mode leakage current, INH pin grounded	INH	I_{INH_Off}	−0.5	—	0.5	µA	A
11.03	Pull-down Resistance in Sleep and VCC Overtemp mode		INH	$R_{INH\_PD\_Sleep}$	175	260	400	kΩ	A
CANH, CANL (see Figure 6-3 for the definition of R_L and the test circuit)									
8.03	Single-Ended Dominant Output Voltage	$R_L = 50Ω$ to $65Ω$	CANH	V_{CANH}	2.75	3.5	4.5	V	B
8.04			CANL	V_{CANL}	0.5	1.5	2.25	V	B

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No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
8.05	Transmitter Voltage Symmetry	$V_{Sym} = (V_{CANH} + V_{CANL})/V_{VCC}$, R_L = 60Ω, C_1 = 4.7 nF, f_{TXD} = 1 MHz	CANH, CANL	V_{SYM}	0.9	—	1.1	V	D
8.06	Dominant Differential Output Voltage	Normal mode, V_{TXD} = 0V, V_{VCC} = 4.7V to 5.5V, $t < t_{to(dom)}$ R_L = 50Ω to 65Ω	CANH, CANL	V_{Diff}	1.5	—	3	V	B
8.07		Normal mode, V_{TXD} = 0V, V_{VCC} = 4.7V to 5.5V, $t < t_{to(dom)}$ R_L = 45Ω to 70Ω	CANH, CANL	V_{Diff}	1.4	—	3.2	V	B
8.08		Normal mode, V_{TXD} = 0V, V_{VCC} = 4.7V to 5.5V, $t < t_{to(dom)}$ R_L = 2240Ω	CANH, CANL	V_{Diff}	1.5	—	5	V	D
8.09	Recessive Output Voltage	Single-Ended output voltage on CANH/CANL, CAN biased, $V_{TXD} = V_{VIO}$, no load	CANH, CANL	V_{CANH}, V_{CANL}	2	0.5 x V_{VCC}	3	V	A
8.10		Single-Ended output voltage on CANH/CANL, CAN unbiased, $V_{TXD} = V_{VIO}$, no load	CANH, CANL	V_{CANH}, V_{CANL}	−0.1	—	0.1	V	A
8.11		Differential output voltage (bus biasing active), no load	CANH, CANL	V_{Diff}	−50	—	50	mV	A
8.12		Differential output voltage (bus biasing inactive), no load	CANH, CANL	V_{Diff}	−50	—	50	mV	A
8.13	Differential Receiver Threshold Voltage	Normal/Receive Only mode; V_{CANL} , V_{CANH} = −12V to +12V	—	$V_{Diff\_rx\_th}$	0.5	0.7	0.9	V	A
8.14		Standby/Sleep mode; V_{CANL} , V_{CANH} = −12V to +12V	—	$V_{Diff\_rx\_th}$	0.4	0.7	1.15	V	B
8.15	Differential Receiver Threshold Voltage	Normal/Receive Only mode; V_{CANL} , V_{CANH} = −27V to +27V	—	$V_{Diff\_rx\_th}$	0.5	0.7	0.9	V	B
8.16		Standby/Sleep mode; V_{CANL} , V_{CANH} = −27V to +27V	—	$V_{Diff\_rx\_th}$	0.4	0.7	1.15	V	B
8.17	Differential Receiver Hysteresis Voltage	Normal/Receive Only mode; V_{CANL} , V_{CANH} = −12V to +12V	—	V_{hys_rx}	50	120	200	mV	B
8.18	Differential Receiver Hysteresis Voltage	Normal/Receive Only mode; V_{CANL} , V_{CANH} = −27V to +27V	—	V_{hys_rx}	50	120	200	mV	B

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No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
8.19	Maximum Driver Output Current	Normal mode, CAN dominant, V_{TXD} = 0, t < $t_{to(dom)}$, V_{VCC} = 5V, V_{CANH} = −5V	—	I_{CANH_max}	−75	—	−33	mA	A
8.20	Maximum Driver Output Current	Normal mode, CAN dominant, V_{TXD} = 0, t < $t_{to(dom)}$, V_{VCC} = 5V, V_{CANL} = 27V	—	I_{CANL_max}	33	—	75	mA	A
8.21	Input Leakage Current	V_{VS} = V_{VCC} = V_{VIO} = 0V, V_{CANH} = V_{CANL} = 5V	—	I_{leak_in} (I_{CANH}, I_{CANL})	−5	—	+5	µA	A
8.22		V_{VS} = V_{VCC} = V_{VIO} shorted to ground through 47 kΩ, V_{CANH} = V_{CANL} = 5V	—	I_{leak_in} (I_{CANH}, I_{CANL})	−5	—	+5	µA	D
8.23	Single-Ended Input Resistance	V_{CANH} = V_{CANL} = 5V	CANH, CANL	R_{CANH}, R_{CANL}	9	15	28	kΩ	A
8.24		−2V ≤ V_{CANH} ≤ 7V, −2V ≤ V_{CANL} ≤ 7V	CANH, CANL	R_{CANH}, R_{CANL}	9	15	28	kΩ	D
8.25	Matching of Internal Resistance Between CANH and CANL	V_{CANH} = V_{CANL} = 5V, mR = 2 × (R_{CANH} - R_{CANL})/(R_{CANH} + R_{CANL})	—	mR	−1	—	1	%	A
8.26		−2V ≤ V_{CANH} ≤ 7V, −2V ≤ V_{CANL} ≤ 7V mR = 2 × (R_{CANH} - R_{CANL})/(R_{CANH} + R_{CANL})	—	mR	−1	—	1	%	D
8.27	Differential Internal Resistance	V_{CANH} = V_{CANL} = 5V	—	R_{Diff}	18	30	56	kΩ	A
8.28		−2V ≤ V_{CANH} ≤ 7V, −2V ≤ V_{CANL} ≤ 7V	—	R_{Diff}	18	30	56	kΩ	D
8.29	Common-Mode Input Capacitance	f = 500 kHz, CANH and CANL referring to ground	—	$C_{i(cm)}$	—	—	20	pF	D
8.30	Differential Input Capacitance	f = 500 kHz, between CANH and CANL	—	C_{Diff}	—	—	10	pF	D
8.31	Differential Bus Voltage Range for Recessive State Detection	Bus biasing active -27V ≤ V_{CANL} ≤ +27V -27V ≤ V_{CANH} ≤ +27V	—	V_{Diff_rec}	−3	—	+0.5	V	D
8.32	Differential Bus Voltage Range for Recessive State Detection	Bus biasing inactive -27V ≤ V_{CANL} ≤ +27V -27V ≤ V_{CANH} ≤ +27V	—	V_{Diff_rec}	−3	—	+0.4	V	D
8.33	Differential Bus Voltage Range for Dominant State Detection	Bus biasing active -27V ≤ V_{CANL} ≤ +27V -27V ≤ V_{CANH} ≤ +27V	—	$V_{DIFF\_dom\_a}$	0.9	—	8	V	D
8.34	Differential Bus Voltage Range for Dominant State Detection	Bus biasing inactive -27V ≤ V_{CANL} ≤ +27V -27V ≤ V_{CANH} ≤ +27V	—	$V_{DIFF\_dom\_i}$	1.15	—	8	V	D
Transceiver Timing, Pins WAKE, INH, CANH, CANL, TXD and RXD. See Figure 6-1, Figure 6-2 and Figure 6-3 for the definition of the timing parameters and the test circuit.									
9.01	Delay Time from TXD to Bus Dominant	R_L = 60Ω, C_L = 100 pF	CANH, CANL, TXD	t_{TXDBUS_dom}	—	—	80	ns	C

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No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
9.02	Delay Time from TXD to Bus Recessive	R_L = 60Ω, C_L = 100 pF	CANH, CANL, TXD	t_{TXDBUS_rec}	—	—	90	ns	C
9.03	Delay Time from bus Dominant to RXD	R_L = 60Ω, C_L = 100 pF	CANH, CANL, RXD	t_{BUSRXD_dom}	20	—	110	ns	C
9.04	Delay Time from Bus Recessive to RXD	R_L = 60Ω, C_L = 100 pF	CANH, CANL, RXD	t_{BUSRXD_rec}	20	—	130	ns	C
9.05	Propagation Delay from TXD to RXD	Normal mode, Rising edge at pin TXD, R_L = 60Ω, C_L = 100 pF, C_{RXD} = 15 pF	TXD, RXD	t_{Loop}	40	—	210	ns	A
9.06	Propagation Delay from TXD to RXD	Normal mode, Falling edge at pin TXD, R_L = 60Ω, C_L = 100 pF, C_{RXD} = 15 pF	TXD, RXD	t_{Loop}	40	—	190	ns	A
9.07	Propagation Delay from TXD to RXD	Normal mode, Rising edge at pin TXD, R_L = 150Ω, C_L = 100 pF, C_{RXD} = 15 pF	TXD, RXD	t_{Loop}	—	—	300	ns	D
9.08	Propagation Delay from TXD to RXD	Normal mode, Falling edge at pin TXD, R_L = 150Ω, C_L = 100 pF, C_{RXD} = 15 pF	TXD, RXD	t_{Loop}	—	—	300	ns	D
9.09	TXD Dominant Time-Out Time	V_{TXD} = 0V, Normal mode	TXD	$t_{to(dom)}$	2.7	—	3.3	ms	B
9.10	Bus Wake-up Time-out Time	Sleep mode	CANH, CANL	t_{Wake}	0.9	—	1.2	ms	A
9.11	CAN Activity Filter Time for Standard Remote Wake-Up Pattern (WUP)	First pulse (after first recessive) and second pulse for wake-up on pins CANH and CANL, Sleep mode	CANH, CANL	t_{Filter}	0.5	—	1.8	µs	A
9.12	Delay Time for Standby mode to Sleep mode Transition	Falling Edge at pin EN and TXD = 0	—	$t_{d\_STBY\_Sleep}$	—	13	20	µs	D
9.13	Delay Time for Normal mode to Sleep mode Transition	Falling edge at pin EN and TXD = 0	—	$t_{d\_Norm\_Sleep}$	—	13	20	µs	D
9.14	Delay Time for Normal mode to Receive Only mode Transition	Falling edge at pin EN and TXD = 1	—	$t_{d\_Norn\_Rec}$	—	3	10	µs	D
9.15	Delay Time for Standby mode to Normal mode Transition	Rising edge at pin EN and TXD = 1	—	$t_{d\_Stby\_Norm}$	—	5	10	µs	D
9.16	Delay Time for Receive Only mode to Silent mode Transition	Rising edge at pin EN and TXD = 0	—	$t_{d\_Rec\_SIL}$	—	14	20	µs	D

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No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
9.17	Delay Time for Silent mode to Standby mode Transition	Falling edge at pin EN and TXD = 1	—	$t_{d\_SIL\_STBY}$	—	13	20	µs	D
9.18	Delay Time for Receive Only mode to Normal mode Transition	Rising edge at pin EN and TXD = 1	—	$t_{d\_Rec\_Norm}$	—	30	50	µs	D
9.19	Delay Time for Sleep mode to Reset mode Transition	EN = 1/WAKE/CAN bus wake-up	—	$t_{d\_Sleep\_Reset}$	—	115	140	µs	D
9.20	Delay Time for OFF mode to Reset mode Transition	$V_{VS} > V_{VS\_PWR\_ON}$	—	$t_{d\_OFF\_Reset}$	—	650	900	µs	D
9.21	TXD to EN mode Select Time		TXD, EN	$t_{d\_mode\_select}$	—	—	3	µs	D
9.22	TXD Lock Time to mode change		TXD	t_{steady_txd}	—	—	60	µs	D
9.23	EN, TXD Lock Time to mode change		EN, TXD	$t_{lock\_mode\_change}$	5	—	—	µs	D
9.24	Time-out Time for Bus Inactivity	Bus recessive time measurement started in Standby mode	CANH, CANL	$t_{Silence}$	0.95	—	1.17	s	B
9.241	Delay Time from Bus Active to Bias on	R_L = 60Ω, C_1 = 4.7 nF, C_L = 0 pF (not present), C_{RXD} = 0 pF (not present)	CANH, CANL	t_{bias}	—	—	200	µs	D
9.25	Debouncing Time for Recessive Clamping State Detection	$V_{(CANH + CANL)} > 900$ mV, RXD = HIGH	RXD	$t_{RXD\_rec\_clmp}$	60	90	175	ns	D
9.26	Debouncing Time for Recessive Clamping State Detection	$V_{(CANH + CANL)} > 900$ mV, RXD = HIGH	RXD	$t_{RXD\_rec\_clmp2}$	—	—	8	µs	D
10.01	Recessive Bit Time on Pin RXD	Normal mode, t_{Bit_TXD} = 500 ns, R_L = 60Ω, C_L = 100 pF, C_{RXD} = 15 pF	RXD	$t_{Bit(RXD)}$	400	—	550	ns	B
10.02		Normal mode, t_{B_TXD} = 200 ns, R_L = 60Ω, C_L = 100 pF, C_{RXD} = 15 pF	RXD	$t_{Bit(RXD)}$	120	—	220	ns	A
10.03		Normal mode, t_{B_TXD} = 125 ns, R_L = 60Ω, C_L = 100 pF, C_{RXD} = 15 pF	RXD	$t_{Bit(RXD)}$	80	—	145	ns	A

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No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
10.04	Transmitted Recessive Bit Width on the Bus	t_{B_TXD} = 500 ns RL = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF	—	$t_{Bit(Bus)}$	450	—	530	ns	B
10.05		t_{B_TXD} = 200 ns RL = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF	—	$t_{Bit(Bus)}$	155	—	210	ns	A
10.06		t_{B_TXD} = 125 ns RL = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF	—	$t_{Bit(Bus)}$	95	—	135	ns	A
10.07	Receiver Timing Symmetry	$\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$, t_{B_TXD} = 500 ns (see no. 9.100 for $t_{Bit(Bus)}$) RL = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF	—	Δt_{Rec}	−65	—	+40	ns	B
10.08		$\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$, t_{B_TXD} = 200 ns RL = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF	—	Δt_{Rec}	−45	—	+15	ns	A
10.09		$\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$, t_{B_TXD} = 125 ns RL = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF	—	Δt_{Rec}	−45	—	+10	ns	A
10.10	Transmitter Resume Time	Minimum pulse width to reset the transmitter after a TXD dominant time-out event	TXD	$t_{TX\_resume\_TXDOUT}$	10	—	—	µs	D

* Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter.

Figure 6-1. CAN Transceiver Timing Diagram 1

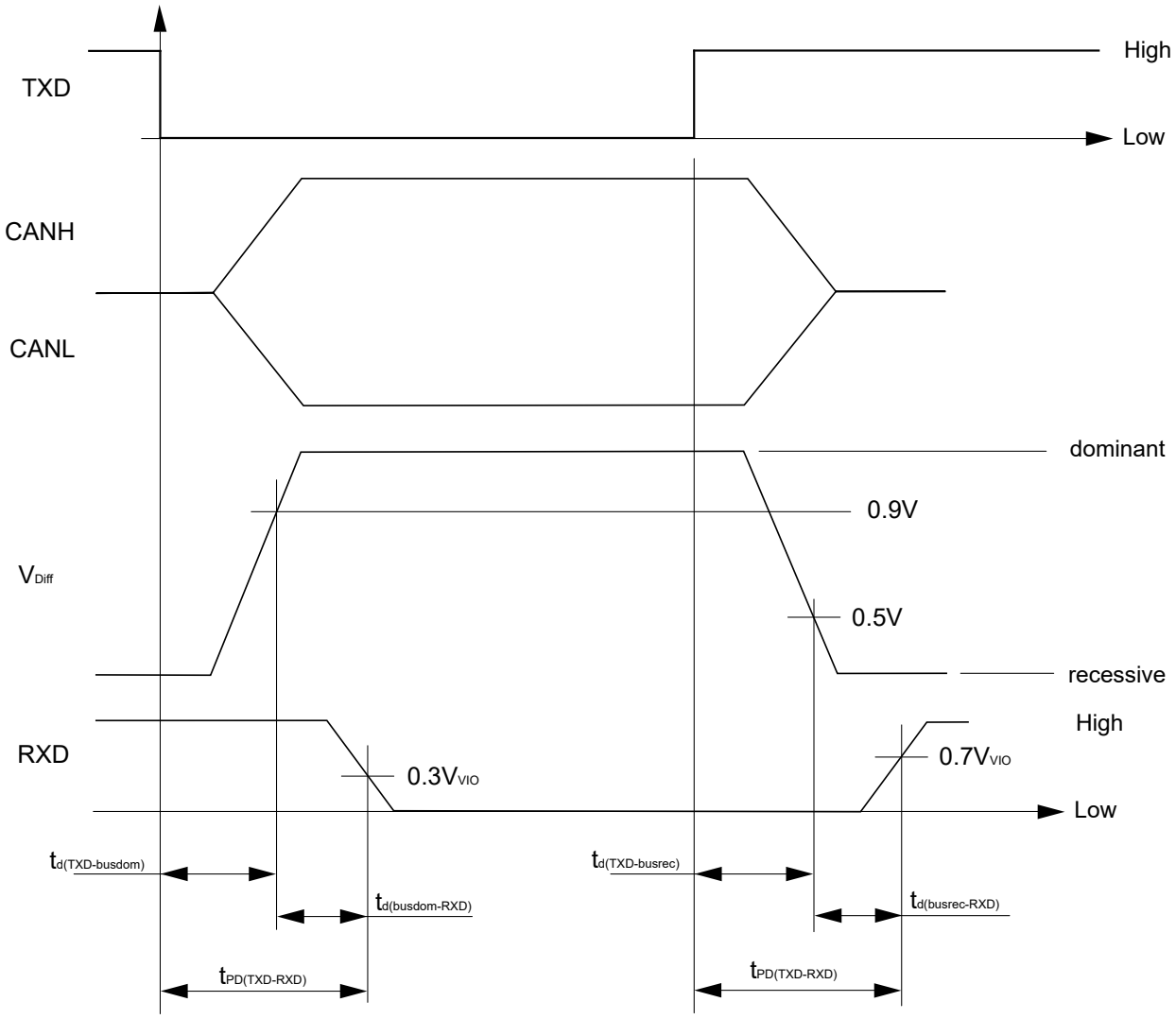


Figure 6-2. CAN Transceiver Timing Diagram 2

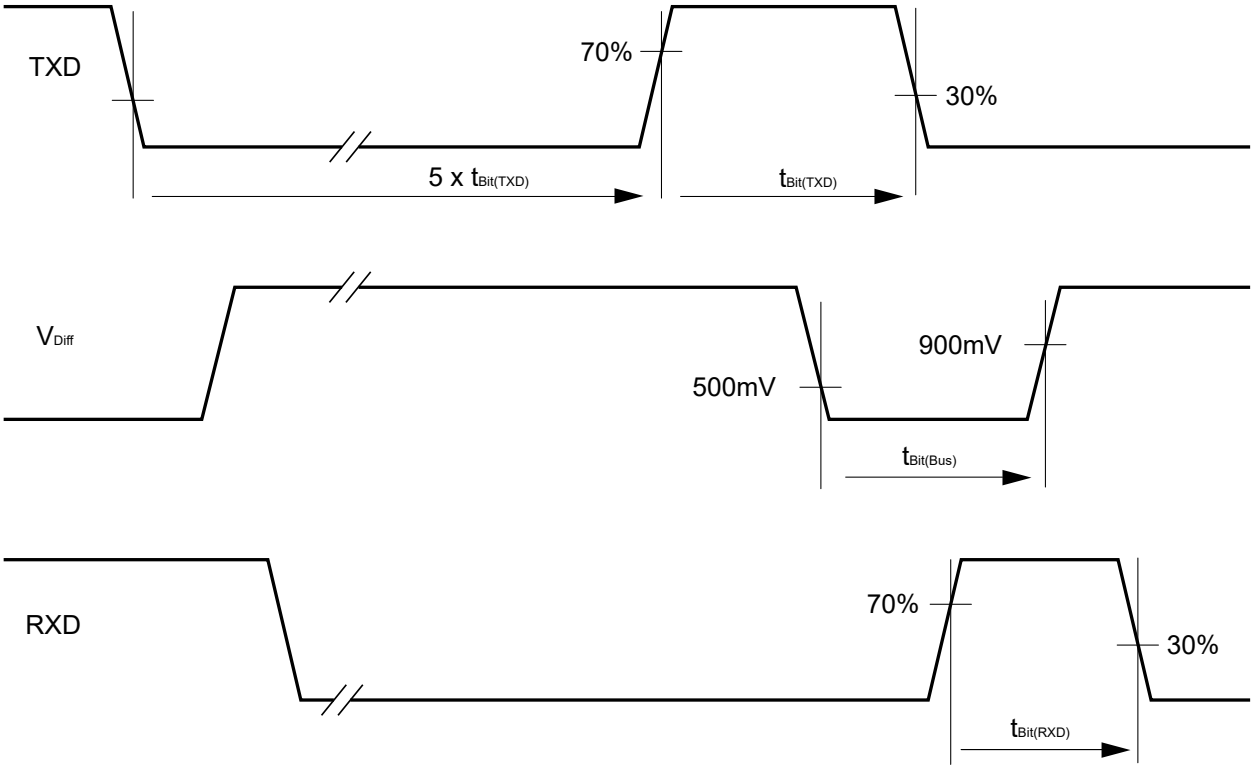
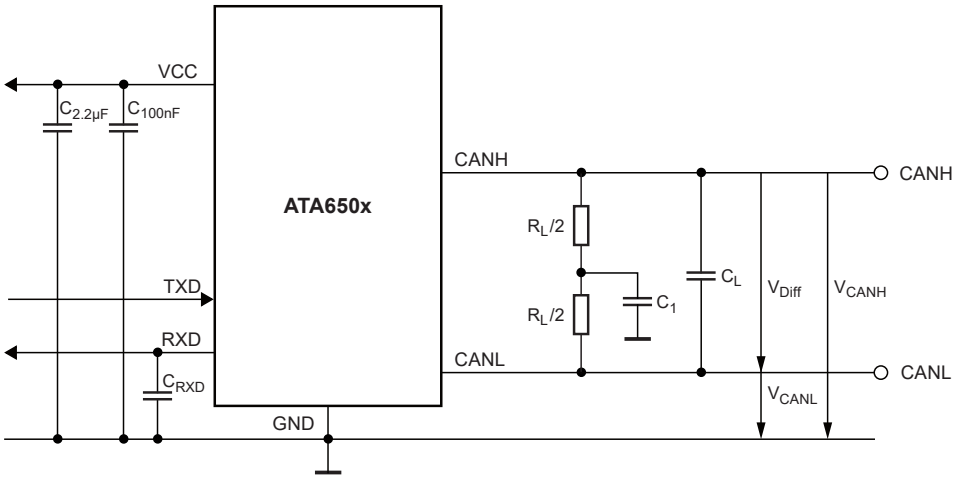


Figure 6-3. Timing Test Circuit



6.3 Thermal Characteristics

Table 6-1. Thermal Characteristics VDFN8

Parameters	Sym.	Min.	Typ.	Max.	Unit
Thermal Resistance Virtual Junction to Heat Slug	R_{thvJC}	—	11	—	K/W
Thermal Resistance Virtual Junction to Ambient, where Heat Slug is soldered to PCB according to JEDEC	R_{thvJA}	—	53	—	K/W
Thermal Shutdown of the Bus Drivers	T_{Jsd}	170	—	195	°C
Thermal Shutdown of the VCC Voltage Regulator	T_{Jsd}	170	—	195	°C
Thermal Shutdown Hysteresis	T_{Jsd_hys}	—	15	—	K

Table 6-2. Thermal Characteristics VDFN10

Parameters	Sym.	Min.	Typ.	Max.	Unit
Thermal Resistance Virtual Junction to Heat Slug	R_{thvJC}	—	10	—	K/W
Thermal Resistance Virtual Junction to Ambient, where Heat Slug is soldered to PCB according to JEDEC	R_{thvJA}	—	50	—	K/W
Thermal Shutdown of the Bus Drivers	T_{Jsd}	170	—	195	°C
Thermal Shutdown of the VCC Voltage Regulator	T_{Jsd}	170	—	195	°C
Thermal Shutdown Hysteresis	T_{Jsd_hys}	—	15	—	K

Table 6-3. Thermal Characteristics VDFN14

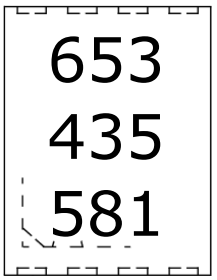
Parameters	Sym.	Min.	Typ.	Max.	Unit
Thermal Resistance Virtual Junction to Heat Slug	R_{thvJC}	—	8	—	K/W
Thermal Resistance Virtual Junction to Ambient, where Heat Slug is soldered to PCB according to JEDEC	R_{thvJA}	—	45	—	K/W
Thermal Shutdown of the Bus Drivers	T_{Jsd}	170	—	195	°C
Thermal Shutdown of the VCC Voltage Regulator	T_{Jsd}	170	—	195	°C
Thermal Shutdown Hysteresis	T_{Jsd_hys}	—	15	—	K

7. Package Information

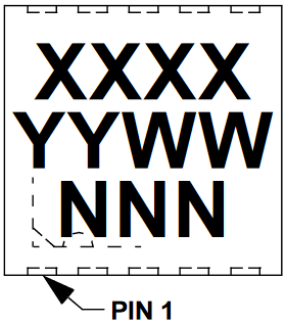
Package Marking Information

8-Lead 2x3mm VDFN

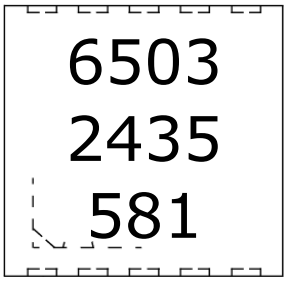
Example



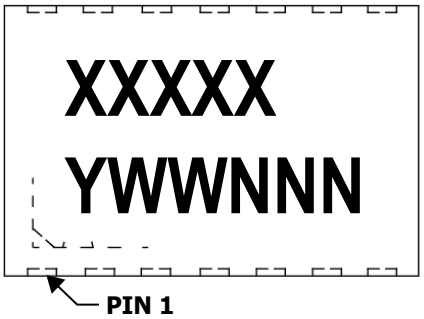
10-Lead 3x3mm VDFN



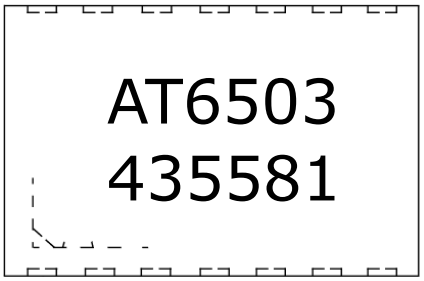
Example



14-Lead 4.5x3mm VDFN



Example

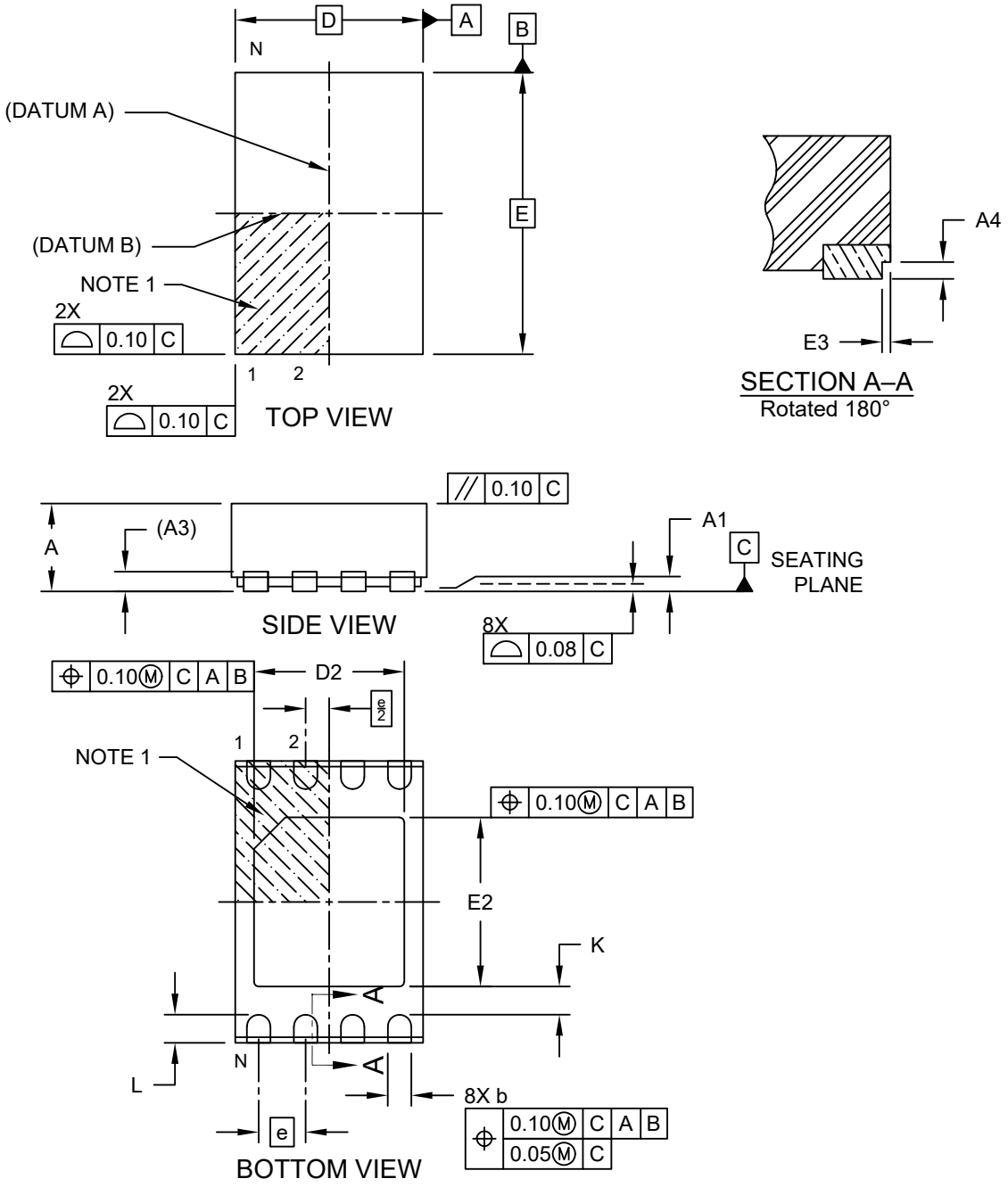


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Very Thin Plastic Dual Flat, No Lead Package (4CW) - 2x3x0.9 mm Body [VDFN] 1.6x1.8 mm Exposed Pad Wettable Step Cut Flanks

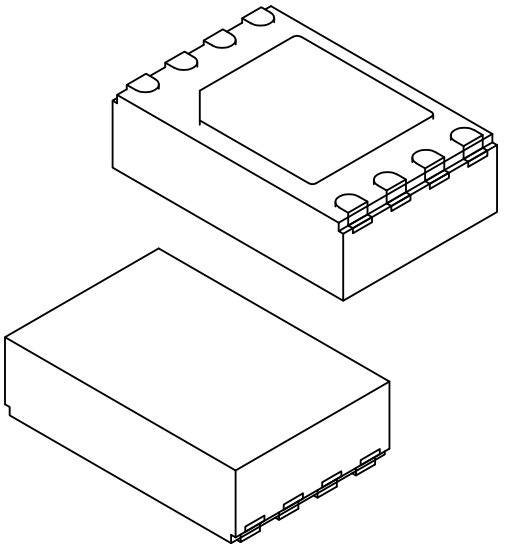
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-581 Rev A Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (4CW) - 2x3x0.9 mm Body [VDFN] 1.6x1.8 mm Exposed Pad Wettable Step Cut Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		008	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.50
Terminal Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.70	1.80	1.90
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.20	0.30	0.40
Terminal-to-Exposed-Pad	K	0.20	–	–
Wettable Flank Step Cut Width	E3	0.035	0.06	0.085
Wettable Flank Step Cut Depth	A4	0.100	–	0.190

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

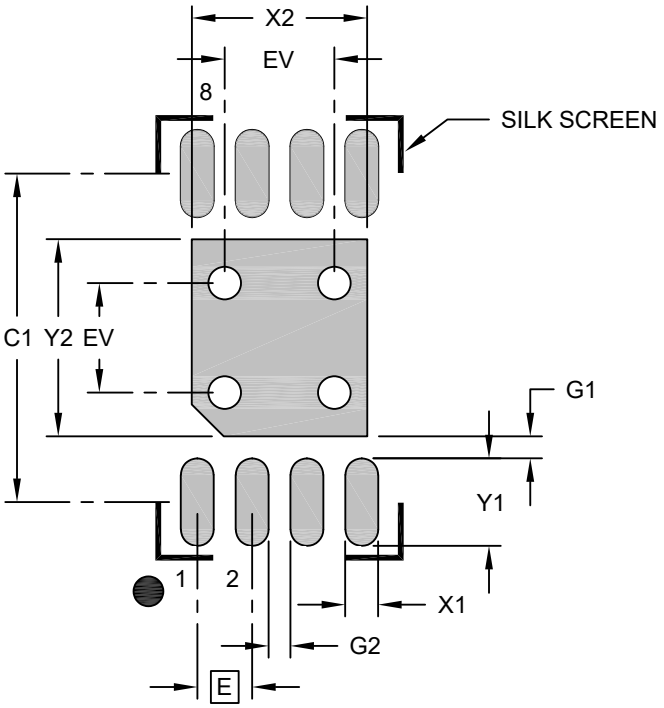
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-581 Rev A Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (4CW) - 2x3x0.9 mm Body [VDFN] 1.6x1.8 mm Exposed Pad Wettable Step Cut Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.80
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

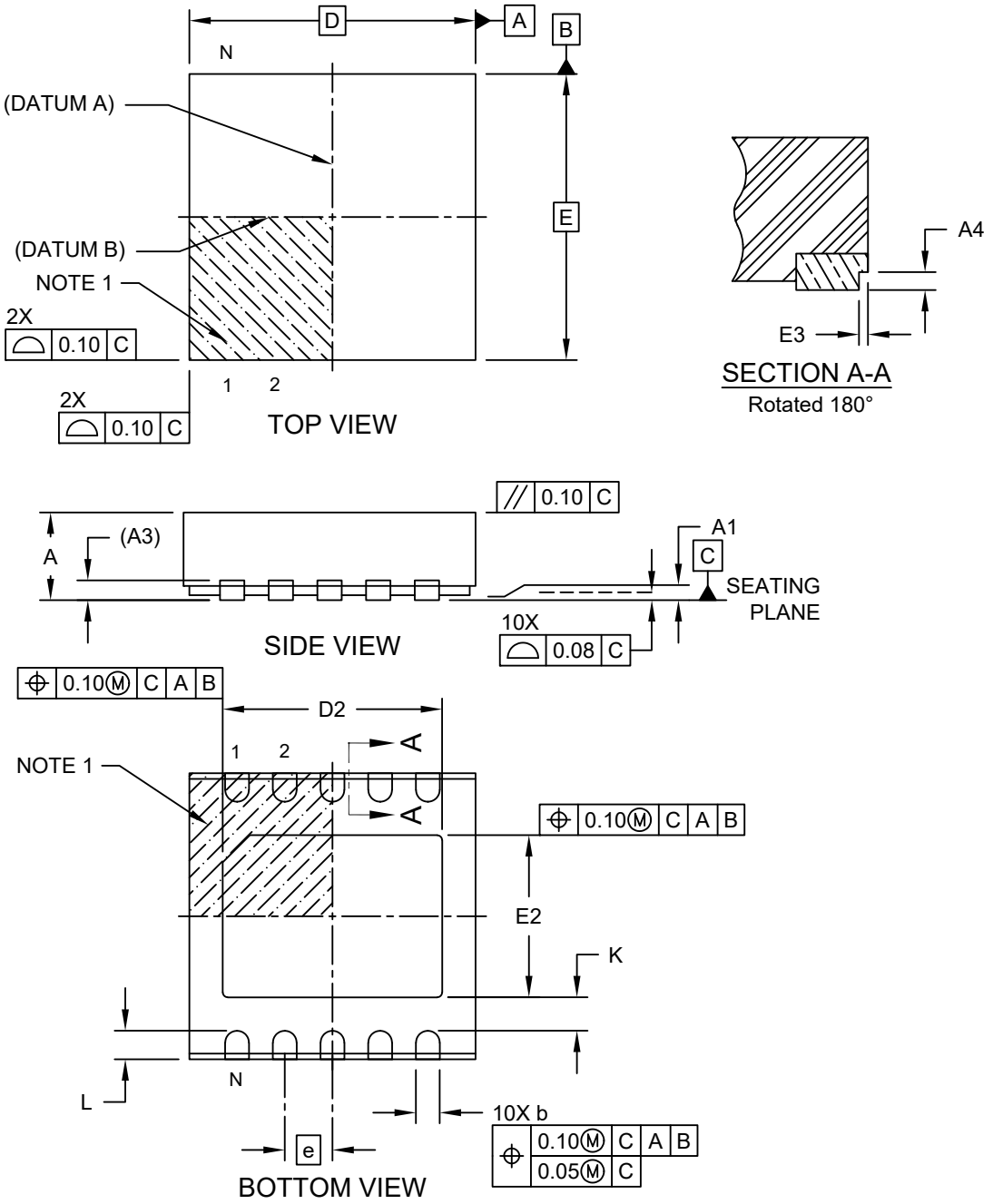
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2581 Rev A

10-Lead Very Thin Plastic Dual Flat, No Lead Package (4BW) - 3x3x0.9 mm Body [VDFN] With 2.3x1.7 mm Exposed Pad and Step Cut Wettable Flanks

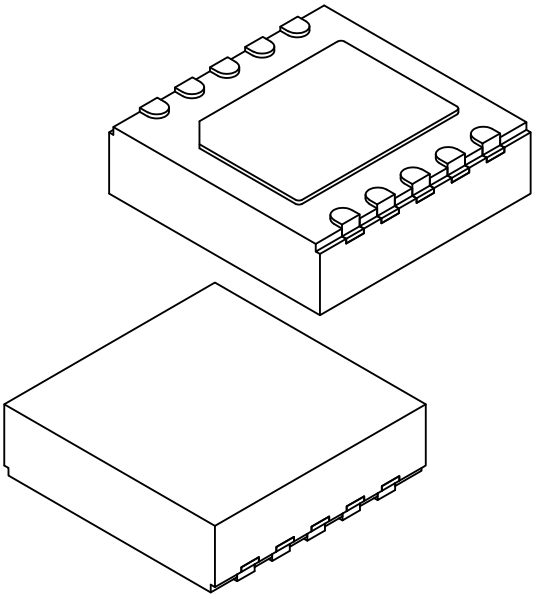
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-580 Rev B Sheet 1 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (4BW) - 3x3x0.9 mm Body [VDFN] With 2.3x1.7 mm Exposed Pad and Step Cut Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.20	2.30	2.40
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.60	1.70	1.80
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.20	0.30	0.40
Terminal-to-Exposed-Pad	K	0.20	–	–
Wettable Flank Step Cut Width	E3	0.035	0.06	0.085
Wettable Flank Step Cut Depth	A4	0.10	–	0.19

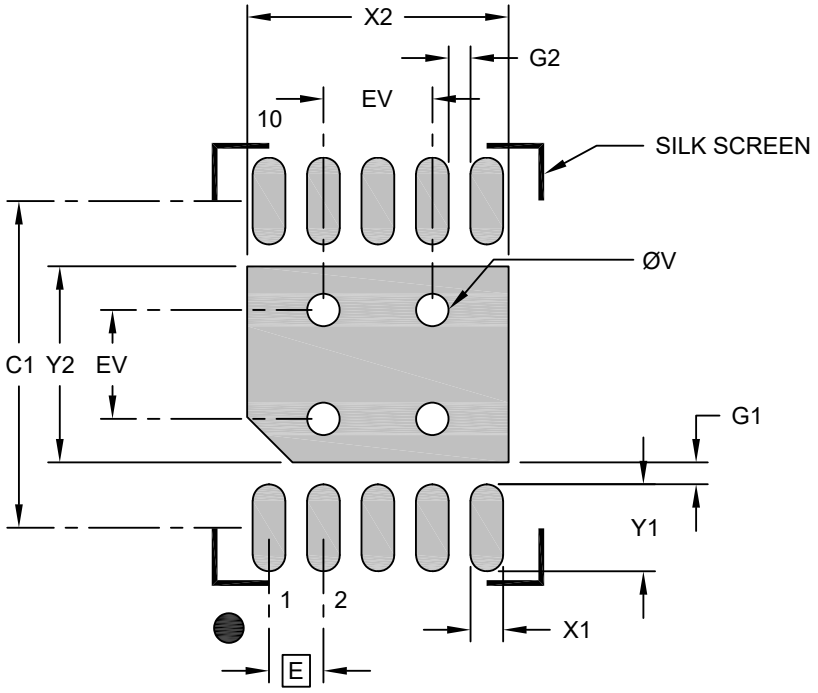
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-580 Rev B Sheet 2 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (4BW) - 3x3x0.9 mm Body [VDFN] With 2.3x1.7 mm Exposed Pad and Step Cut Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			2.40
Center Pad Length	Y2			1.80
Contact Pad Spacing	C1		3.00	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.80
Contact Pad to Center Pad (Xnn)	G1	0.20		
Contact Pad to Contact Pad (Xnn)	G2	0.25		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

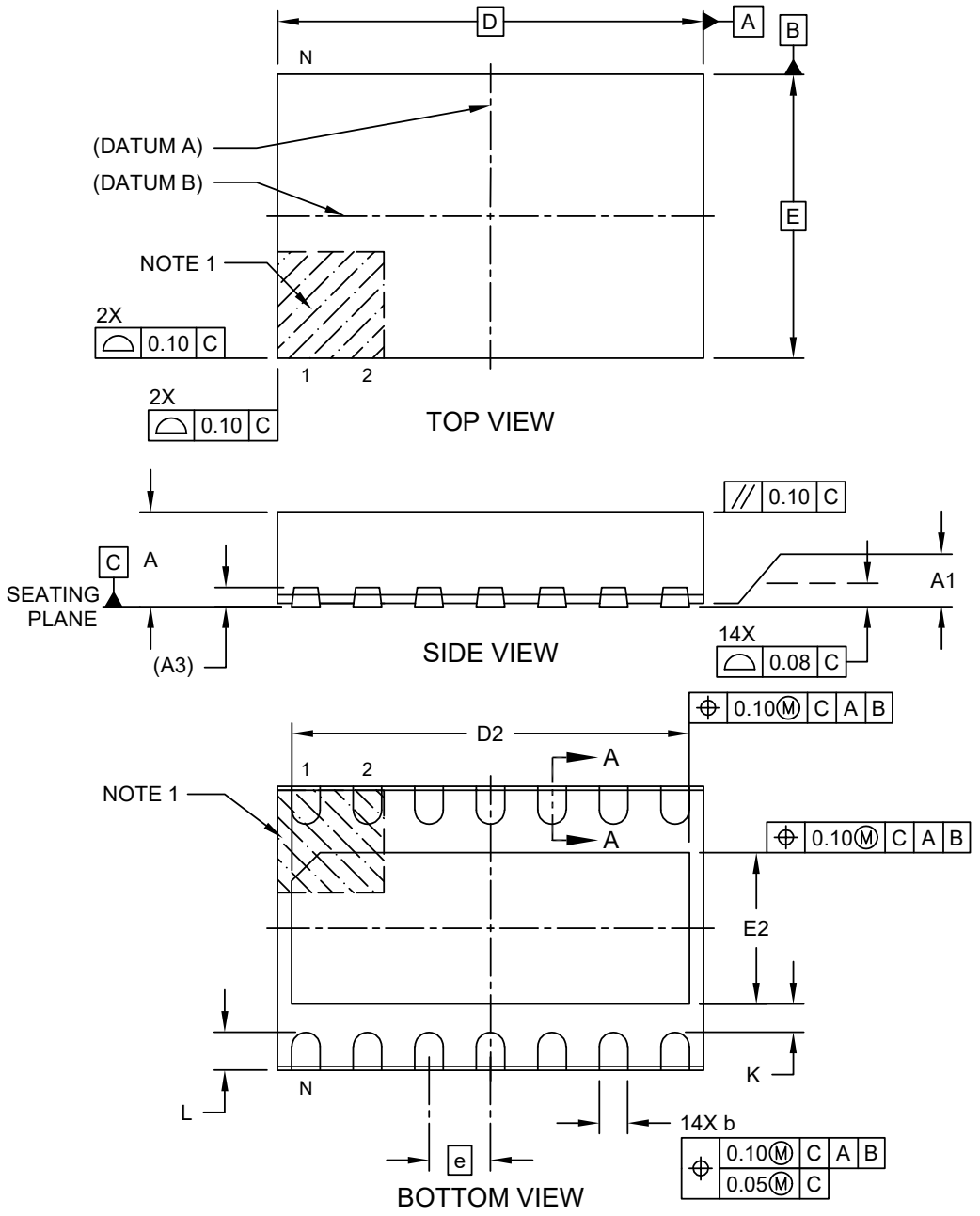
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2580 Rev B

14-Lead Very Thin Plastic Dual Flat, No Lead Package (QBB) - 4.5x3x1 mm Body [VDFN] With 1.6x4.2 mm Exposed Pad and Stepped Wettable Flanks

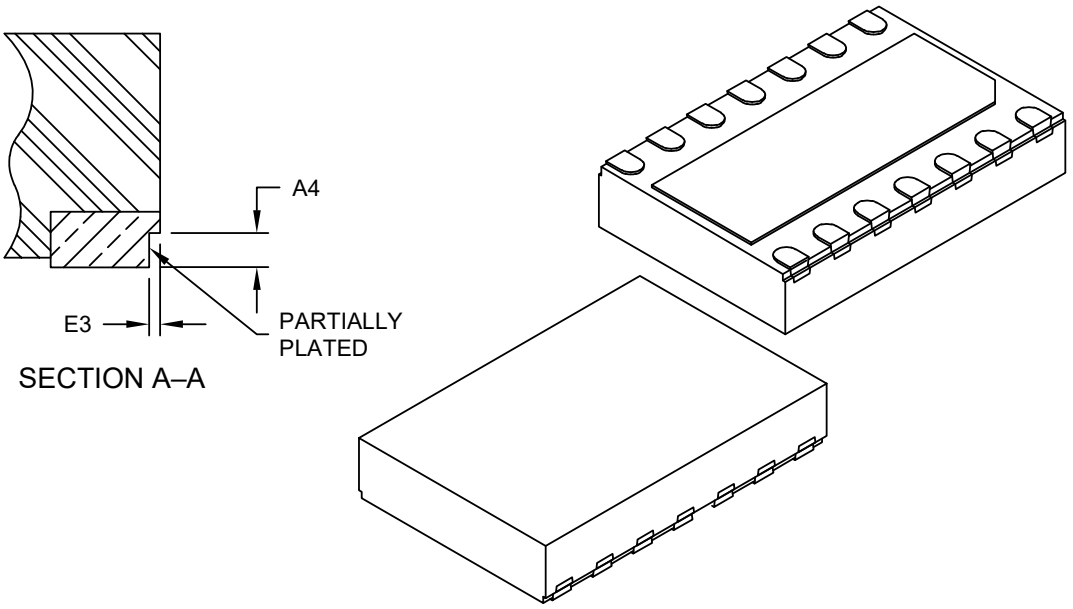
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21361 Rev D Sheet 1 of 2

14-Lead Very Thin Plastic Dual Flat, No Lead Package (QBB) - 4.5x3x1 mm Body [VDFN] With 1.6x4.2 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.03	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		4.50 BSC	
Exposed Pad Length	D2	4.15	4.20	4.25
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.27	0.32	0.37
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Depth	A4	0.10	-	0.19
Wettable Flank Step Cut Width	E3	-	-	0.085

Notes:

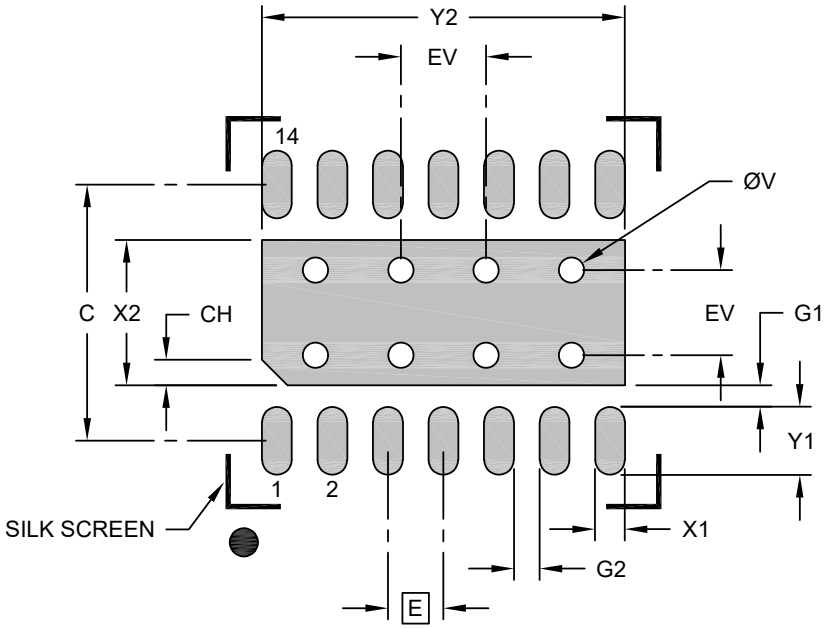
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21361 Rev D Sheet 2 of 2

14-Lead Very Thin Plastic Dual Flat, No Lead Package (QBB) - 4.5x3x1 mm Body [VDFN] With 1.6x4.2 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			4.25
Contact Pad Spacing	C		3.00	
Contact Pad Width (X14)	X1			0.35
Contact Pad Length (X14)	Y1			0.80
Pin 1 Index Chamfer	CH		0.30	
Contact Pad to Center Pad (X14)	G1	0.20		
Contact Pad to Center Pad (X12)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23361 Rev D

8. Revision History

Revision A (July 2024)

Original Release of this Document.

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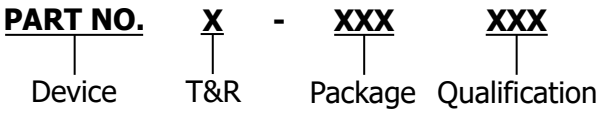

Device:	ATA6500	VDFN8 High-Speed CAN FD Transceiver for 1.8V and 5V I/O support
	ATA6501	VDFN8 High-Speed CAN FD Transceiver for 3.3V and 5V I/O support
	ATA6502	VDFN10 High-Speed CAN FD Transceiver for 1.8V and 5V I/O support
	ATA6503	VDFN10 High-Speed CAN FD Transceiver for 3.3V and 5V I/O support
	ATA6504	VDFN14 High-Speed CAN FD Transceiver for 1.8V and 5V I/O support
	ATA6505	VDFN14 High-Speed CAN FD Transceiver for 3.3V and 5V I/O support
Tape and Reel option:	T	330 mm diameter Tape and Reel
Package:	4CW	8-Lead VDFN with Wettable Flanks (Moisture Sensitivity Level 1)
	4BW	10-Lead VDFN with Wettable Flanks (Moisture Sensitivity Level 1)
	QBB	14-Lead VDFN with Wettable Flanks (Moisture Sensitivity Level 1)
Qualification:	VAO	Automotive

- ATA6500T-4CWVAO – High-Speed CAN FD Transceiver with 5V LDO, 1.8V I/O support, VDFN8 package, Tape and Reel, Grade 0, Automotive qualified
- ATA6501T-4CWVAO – High-Speed CAN FD Transceiver with 5V LDO, 3.3V and 5V I/O support, VDFN8 package, Tape and Reel, Grade 0, Automotive qualified
- ATA6502T-4BWVAO – High-Speed CAN FD Transceiver with 5V LDO, 1.8V I/O support, VDFN10 package, Tape and Reel, Grade 0, Automotive qualified
- ATA6503T-4BWVAO – High-Speed CAN FD Transceiver with 5V LDO, 3.3V and 5V I/O support, VDFN10 package, Tape and Reel, Grade 0, Automotive qualified
- ATA6504T-QBBVAO – High-Speed CAN FD Transceiver with 5V LDO, 1.8V I/O support, VDFN14 package, Tape and Reel, Grade 0, Automotive qualified
- ATA6505T-QBBVAO – High-Speed CAN FD Transceiver with 5V LDO, 3.3V and 5V I/O support, VDFN14 package, Tape and Reel, Grade 0, Automotive qualified
- ATA6500T-4CW – High-Speed CAN FD Transceiver with 5V LDO, 1.8V I/O support, VDFN8 package, Tape and Reel, Grade 0
- ATA6501T-4CW – High-Speed CAN FD Transceiver with 5V LDO, 3.3V and 5V I/O support, VDFN8 package, Tape and Reel, Grade 0
- ATA6502T-4BW – High-Speed CAN FD Transceiver with 5V LDO, 1.8V I/O support, VDFN10 package, Tape and Reel, Grade 0
- ATA6503T-4BW – High-Speed CAN FD Transceiver with 5V LDO, 3.3V and 5V I/O support, VDFN10 package, Tape and Reel, Grade 0
- ATA6504T-QBB – High-Speed CAN FD Transceiver with 5V LDO, 1.8V I/O support, VDFN14 package, Tape and Reel, Grade 0
- ATA6505T-QBB – High-Speed CAN FD Transceiver with 5V LDO, 3.3V and 5V I/O support, VDFN14 package, Tape and Reel, Grade 0

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.
3. RoHS compliant, maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (CI) and less than 0.15% (1500) total Bromine (Br) and Chlorine (CI) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.

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